Back-End-of-Line and Micro-C4 Thermal Resistance Contributions to 3-D Stack Packages

Jamil Wakil, Evan G. Colgan, *Senior Member, IEEE*, and Shaochen Chen

***Abstract*— The objective of this paper is to understand and quantify the additional thermal resistance of 3-D stacked packages due to the back-end-of-line (BEOL) layers and die-to-die interconnects, specifically micro-C4s. Of particular interest were the impacts of through silicon vias (TSVs), interfacial thermal resistances between BEOL material layers, and mechanical strain. The study revealed that the TSVs could be effective in reducing overall thermal resistance given an adequately small pitch, alignment with micro-C4s, and penetration through the BEOL layers. A review of theoretical and experimental studies by others revealed vastly different results for the interfacial thermal resistance between material layers, such as in BEOL layers. Theoretical studies suggested 1–2 orders of magnitude lower thermal resistance than experiments. Analysis of the mechanical strain suggested a difficult to quantify but negligibly small impact on the thermal resistance of BEOL layers.**

***Index Terms*— 3-D stack packaging, back-end-of-line, interfacial resistance, micro-C4, strain, thermal, through silicon via.**

I. Introduction

MUCH of the previous thermal analysis on back-end-of-line (BEOL) layers has been focused on the joule heating in small scale interconnects. The BEOL layers consist of metal and dielectric interconnect layers between the transistors and C4s. The BEOL layers typically consist of alternating layers of lines and vias. BEOL layers can number 1 or 2 for simple designs, and up to 15 or more for large processors. A new concern that has arisen with the advent of 3-D flip-chip stack packages is the additional BEOL layers and die–die interconnect thermal resistances in the primary heat flow path, as shown in Fig. 1. The figure depicts a worst case thermal scenario where a high-powered processor is placed below the memory die which contacts the heat sink. Heat dissipation and power/signal delivery have conflicting needs in package design. While it is advantageous to put the processor next to heat sink to dissipate heat, it is electrically advantageous to have the processor as close to the package carrier as possible. This makes power delivery easier and reduces signal paths while still being able to easily access memory above. However, in addition to the thermal interface material (TIM) resistance between the upper die and heat sink, there is now an additional thermal resistance due to the BEOL layers of the upper die and interconnects between the dies. For this paper, the interconnects between the dies are assumed to be micro-C4s (similar to traditional C4s but typically less than 40 μm in diameter and 20 μm tall). The overall objective of the study in this paper is to identify and quantify the subcomponents of this die–die thermal resistance (R_{dd}) composed of the BEOL and micro-C4 layers.

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J. Wakil and E. G. Colgan are with the IBM Corporation, New York, NY 10504 USA (e-mail: jwakil@us.ibm.com; ecolgan@us.ibm.com).

S. Chen is with the University of Texas at Austin, Austin, TX 78712 USA (e-mail: shaochen.chen@engr.utexas.edu).

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II. BEOL Layer Thru-Plane Thermal Resistance

A previous modeling study by the authors [1] attempted to quantify the BEOL layer thermal resistance. Four pairs of BEOL layers were modeled as shown in Fig. 2. The structures of the interconnect lines and vias were varied, keeping material properties constant. Eleven different designs were modeled, the results of which are shown in Table I. The total metal fraction, as well as the metal fraction for the line and via layers (individually), is specified. Of particular interest were cases where the metal fractions were the same but gave different thermal resistances based on the via/line distribution (i.e., A2 and B2). The finite element method (FEM) results were compared with values obtained using the Maxwell model (1) and the parallel series approximation (2) [2]

$$\frac{k_{eff}}{k_a} = C_o + C_1\Phi_b + C_2\Phi_b^2 + C_3\Phi_b^3 + \ldots \tag{1}$$

$$\left(\frac{L}{K}\right)_{eff} \approx N\left(\frac{L_{lines}}{\Phi_{lines}^{met}k_{lines}^{met} + \Phi_{lines}^{diel}k_{lines}^{diel}}\right) + V\left(\frac{L_{vias}}{\Phi_{vias}^{met}k_{vias}^{met} + \Phi_{vias}^{diel}k_{vias}^{diel}}\right) \tag{2}$$

where Φ is the volume fraction, k the conductivity, N the number of line layers, V the number of via layers, and L the thickness of respective layers. The Maxwell model constants $C_0, C_1, C_2\ldots$ are obtained from fitting the finite element results and are inherently design-specific, whereas the parallel/series approximation uses no design information other than material fractions.

Fig. 3 plots the percent error from the FEM results for the thermal resistance calculated by the Maxwell model (1) and the parallel/series approximation (2). The results suggest that simple averaging schemes without accounting for geometric details would not be sufficiently accurate representations for the BEOL layer thermal resistance.

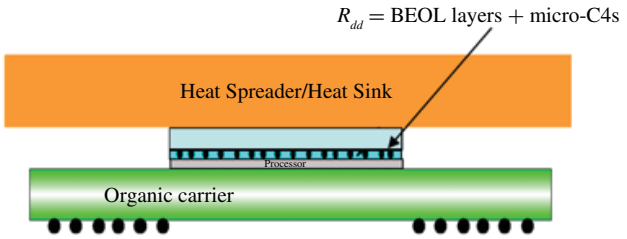

Fig. 1. Schematic of 3-D stacked flip-chip package with high-powered processor below memory layer.

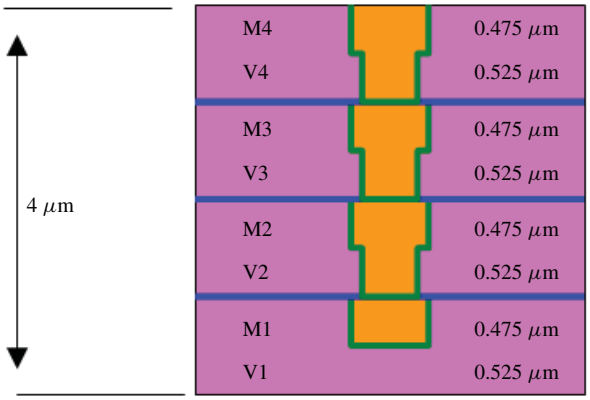

Fig. 2. Four-pair BEOL layers modeled to evaluate effective thermal resistance of the stack for different geometries and metal fractions. M refers to metal (line) layer and V to via layer. Reproduced from [1].

III. Micro-C4 Thermal Resistance

The micro-C4 joint is similar to the traditional C4 solder joint technology except it is scaled down to meet the electrical I/O requirements. The joints can be encapsulated in underfill epoxy for improved cycling reliability. Previous thermal studies of micro-C4s are limited but include Lloyd [3] who measured thermal conductivity and diffusivity of lead-free solder using an iterative inverse method. Szekely [4] used structure functions for a cylindrical heat propagation scenario to model solder joint heat propagation.

The ANSYS software was used to model a micro-C4 unit cell. The objective was to compare the FEM results to a parallel/series thermal resistance model. The ANSYS model is shown in Fig. 4. The model consisted of a single solder joint and the surrounding underfill layer. Also modeled were 5-μm layers with effective conductivities of 15 W/mK in-plane and 1.0 out of plane, which represented BEOL layer stacks on prescribed sides of the joints. For the face-to-face joining condition (in which the active sides of each die would be facing each other), one BEOL layer stack was modeled on each side of the joint. For the face-to-back condition (in which the active side of one die would be attached to the back side of the other), only one BEOL layer stack was modeled on one side of the joint. A no-BEOL layer case was also modeled. One hundred micrometers of silicon was modeled to represent the die on each side of the joint. The thermal resistance of the joint was calculated by finding the total thermal resistance of the structure, and then subtracting the silicon and BEOL layer contributions. For this particular analysis, highly accurate

TABLE I
Thermal Resistance of Four-Pair BEOL Layers for Different Configurations of Vias and Lines. $I_{diel} = 0.54$ W/mK, $I_{met} = 380$ W/mK. From [1]

Case	Vias Desc	Lines/Space	Metal fraction: Total/Line layer/ via layer	%Via Area	Out of Plane Resistance
A1	Stacked	0.28/0.28 μm	0.239/.5/.0031	0.31	2.9 Cmm^2/W
A2	Stacked	0.28/0.28 μm	0.262/.5/.0625	6.25	1.2
B1	Connected staggered	0.28/0.28 μm	0.239/.5L/.0031	0.31	2.6
B2	Connected staggered	0.28/0.28 μm	0.262/.5/.0625	6.25	1.3
C1	Isolated staggered	0.28/0.28 μm	0.239/.5/.0031	0.31	3.6
C2	Isolated staggered	0.28/0.28 μm	0.262/.5/.0625	6.25	1.8
D1	Isolated staggered	0.28/1.4 μm	0.081/.167/.0031	0.31	4.9
E1	No vias	0.28/1.4 μm	0.079/.167/0	NA	5.7
E2	No vias	0.28/0.28 μm	0.239/.5/0	NA	4.1
F1	Stacked (small spacing)	0.28/0.28 μm	0.24/.5/.0069	0.69	2.9
F2	Stacked (small spacing)	0.28/0.28 μm	0.24/.5/.0069	0.69	3.0

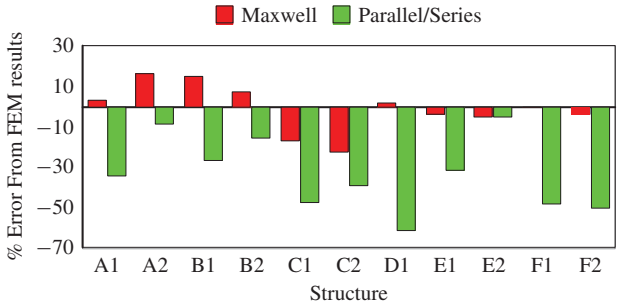

Fig. 3. Percent error from FEM results for the Maxwell and parallel/series models.

properties for the surrounding BEOL layer stack and Si were not so important since only their influence on the micro-C4 layer is investigated. The parallel thermal resistance model was the single layer version of (2).

Fig. 5 shows plots of the micro-C4 thermal resistance as a function of (a) the underfill conductivity and (b) the solder joint conductivity for 100 and 50 μm pitches, respectively, with different BEOL layer configurations. Also shown are the no-BEOL-layer case as well as the parallel/series approximations which obviously do not take into account the surrounding BEOL layers. The results reveal significant difference between the face-to-face, face-to-back, and no-BEOL-layers configurations. This is due primarily to the spreading thermal resistance created by the BEOL layers. The main conclusion is that the BEOL layers adjacent to the micro-C4 greatly impacts the results and that independent analysis of the micro-C4 and BEOL layers is not possible. Subsequent analysis will include

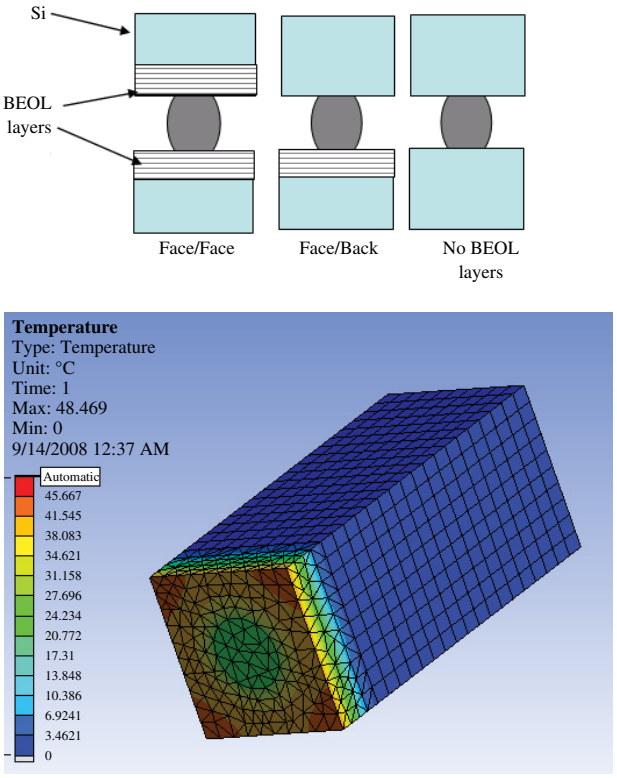

Fig. 4. Structures modeled (top) ANSYS thermal model of a micro-C4 unit cell, showing (bottom) one side of the model.

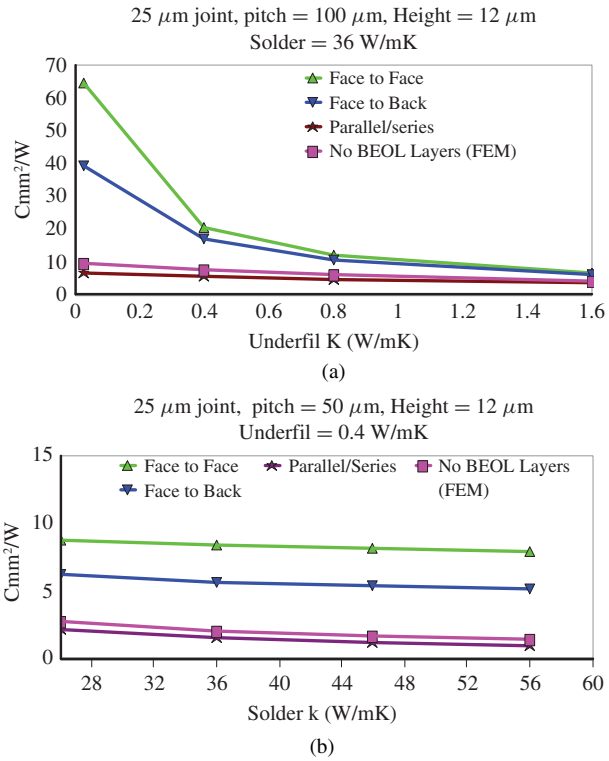

Fig. 5. Micro-C4 thermal resistance as a function of (a) underfill conductivity and (b) solder conductivity for different micro-C4 pitches and BEOL layer configurations.

the BEOL layers, underfill, and micro-C4 thermal resistance together as R_{dd} (die–die thermal resistance).

IV. Impact of Thru Silicon vias (TSVs)

An important design feature that affects BEOL layer and micro-C4 thermal resistance is the TSV. TSVs are designed for power delivery or signal I/O and can penetrate one or more layers of the BEOL, as shown in Fig. 6. The goal of this section is to determine the impact of the TSV on the thermal resistance of the BEOL layers and micro-C4 layers. As concluded from the previous section, micro-C4 thermal resistance is strongly dependent on the adjacent BEOL layer thermal resistance, and therefore the two features cannot be analyzed separately. The TSVs analyzed in this paper are 20-μm diameter Cu cylinders. Two categories of TSVs exist in industry: fine pitch die-to-die and coarse pitch die-to-ball. These have fundamentally different requirements, manufacturing processes, and minimum pitches. The geometry analyzed in this paper would represent somewhat of an intermediate case between fine and coarse pitch, but more representative of the coarse pitch, especially when aligned with the micro-C4s. The International Technology Roadmap for Semiconductors predicts minimum pitches for coarse pitch TSVs to be ~80 μm by 2015 [5].

A simple four-layer BEOL with micro-C4 layer was modeled in ANSYS, as shown in Fig. 7. The model was used to compare the four-layer BEOL with TSVs penetrating various numbers of layers and aligned with the miroC4 versus non-aligned. Additional Si layers were modeled, on which heat source and heat sink boundary conditions were applied. The

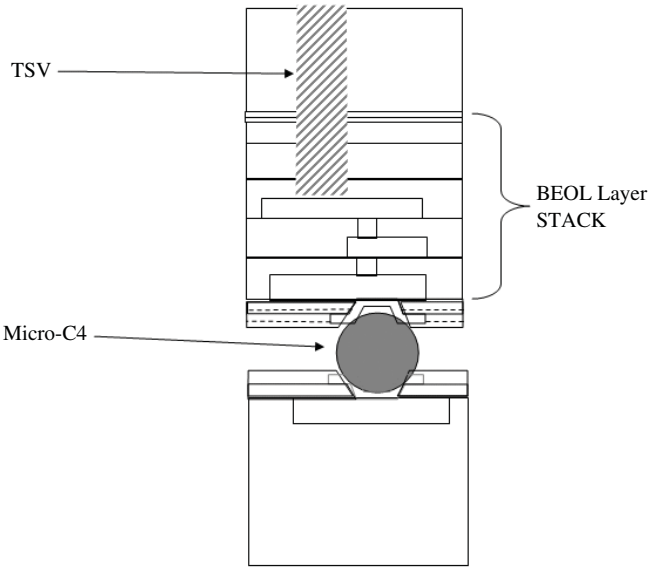

Fig. 6. Example die stack with micro-C4 and TSV penetrating a portion of the BEOL layer stack.

thermal resistance of these silicon layers was subtracted from the total to get the BEOL + micro-C4 composite thermal resistance R_{dd}. The geometry would represent a face-to-back design as described in the previous section.

Fig. 8 shows R_{dd} as a function of the TSV pitch. The micro-C4s are assumed 14 μm tall, 18 μm in diameter, with an underfill conductivity of 1 W/mK. The TSVs are assumed to be not directly aligned with the micro-C4s. The legend

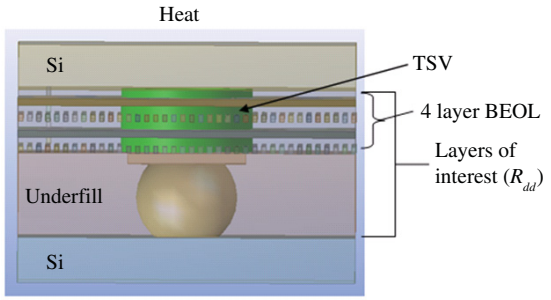

Fig. 7. BEOL layers and micro-C4 model used to evaluate the effect of TSVs.

	Line/space	Line height	Via layer height
Fat	0.8 μm	1.2 μm	1.6 μm
Thin	0.14 μm	0.25 μm	0.25 μm

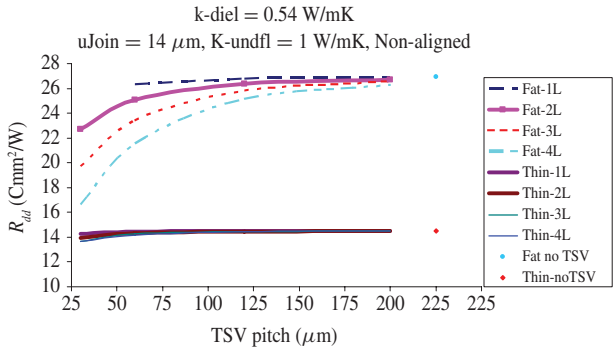

Fig. 8. BEOL layers + micro-C4 thermal resistance (R_{dd}) as a function of TSV pitch for TSVs not aligned with the micro-C4. Micro-C4 solder conductivity is assumed 36 W/mK, and the TSV conductivity is assumed 380 W/mK.

designates the size of lines/spaces modeled and the number of layers the TSV penetrates. Fat-1L designates fat layers with one layer of TSV penetration. The table above the plot shows the dimensions used for fat and thin layers. The dots indicate the infinite TSV pitch (no TSVs). The first observation from Fig. 8 is that the TSV pitch primarily affects the larger fat layers. The second observation is that, beyond ~150 μm pitch, the TSVs become basically ineffective in providing thermal enhancement.

Fig. 9 shows R_{dd} as a function of the dielectric thermal conductivity with fat layers, of 200 μm TSV pitch, 14 μm micro-C4 height, and 1 W/mK underfill conductivity. The TSVs are nonaligned with the micro-C4s. The three curves compare TSV through all four layers, 5% area of micro-vias connecting the layers, and no TSV or vias. The main conclusion is that 5% micro-vias without TSVs is significantly better than having TSVs at this large pitch. It must be noted that the TSV at 200 μm pitch equates to less than 1% Cu. The second observation is that the dielectric conductivity in this range has minimal effect on the structures with 5% vias.

Figs. 10 and 11 compare aligned versus non-aligned TSVs for two and four layer TSV penetrations, for 200 and 30 μm TSV pitches, respectively. The main observation is that the four-layer penetration aligned (with micro-C4) TSV is the only significantly different result. At the larger pitch,

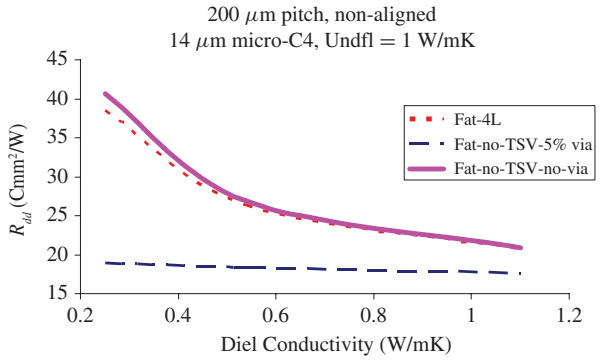

Fig. 9. BEOL Layers + micro-C4 thermal resistance (R_{dd}) as a function of dielectric conductivity for 200-μm TSV pitch, with 14-μm tall micro-C4s and an underfill conductivity of 1W/mK. Micro-C4 solder conductivity is assumed 36 W/mK, and TSV and micro-via conductivity is assumed 380 W/mK.

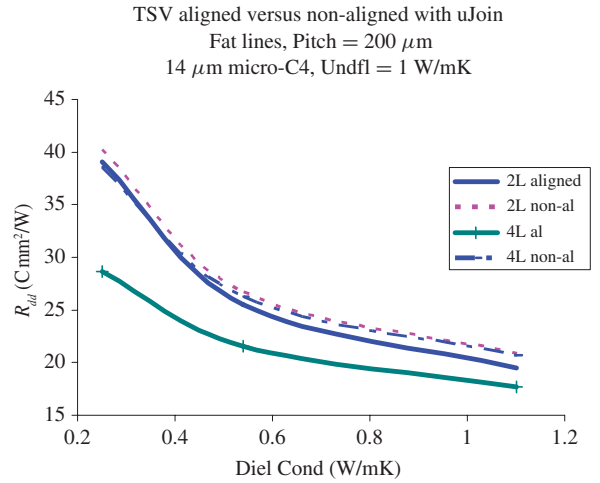

Fig. 10. BEOL layers + micro-C4 thermal resistance (R_{dd}) as a function of dielectric conductivity for 200 μm TSV pitch, with 14-μm tall micro-C4s and an underfill conductivity of 1 W/mK. Micro-C4 solder conductivity is assumed 36 W/mK and metal/TSV conductivity is assumed 380 W/mK.

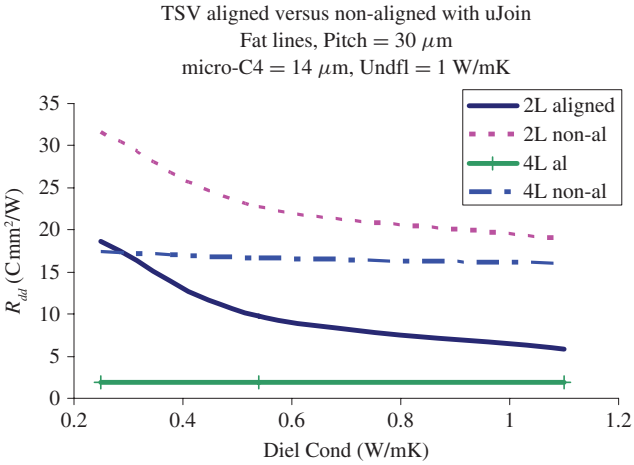

Fig. 11. BEOL Layer + micro-C4 thermal resistance (R_{dd}) as a function of dielectric conductivity for 30 μm TSV pitch, with 14-μm tall micro-C4s and an underfill conductivity of 1 W/mK. Micro-C4 solder conductivity is assumed 36 W/mK and metal/TSV conductivity is assumed 380W/mK.

all the non-fully-penetrated TSV cases are approximately the same regardless of the TSV alignment. The difference is more obvious for the smaller pitch of Fig. 11. Here, one can see

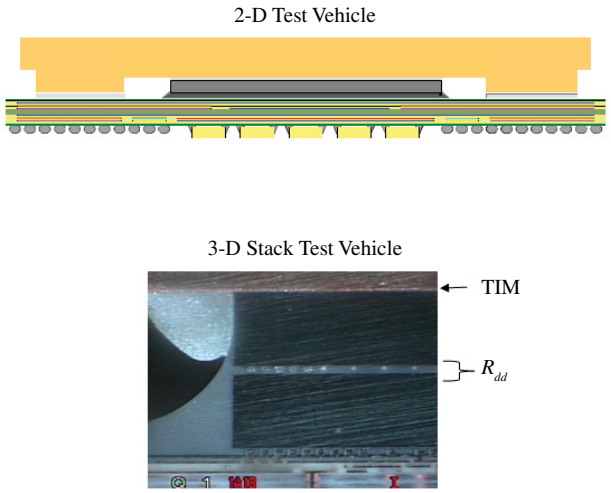

Fig. 12. 2-D test vehicle and cross section of 3-D stack test vehicle used to extract R_{dd} for 70-μm tall C4s, 200 μm pitch with underfill.

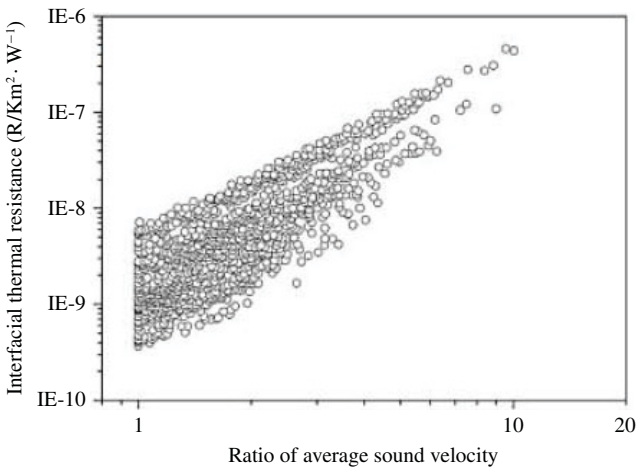

Fig. 13. Interfacial thermal resistance as a function of the ratio of average sound velocities for various material pairs. Reprinted with permission from [8].

TABLE II
MEASUREMENTS OF THETA-jc (LOWER DIE CENTER SENSOR TO LID TOP) AND R_{dd} CORRELATED WITH ANSYS MODEL FOR THE 3-D STACK TEST VEHICLE SHOWN IN FIG. 12

	Measured theta-jc	TIM1 resistance extracted from package model	R_{dd} extracted assuming same TIM1 resistance as the 2-D Pkg.
2-D Test vehicle	19 C mm^2/W	12 C mm^2/W	
3-D Stack test vehicle	102 C mm^2/W		95 C mm^2/W

that the ranking of lowest to highest thermal resistance is: 1) four-layer penetrated aligned TSV; 2) two-layer aligned; 3) four-layer nonaligned; and 4) two-layer nonaligned.

Measurement results on a stacked test vehicle containing two die, with an interface consisting of 200-μm pitch 70-μm tall underfilled C4 joints were used as a rough validation of Figs. 8–11. Fig. 12 shows the test vehicle and cross section, revealing the die stack. The BEOL stack of the top die consisted of five layers. The lower die contained heaters and sensors which could be powered to measure temperatures on the lower die, and a thermocouple was used to measure the lid temperature. The upper die in the 3-D stack TV was not electrically connected but merely attached without reflowing the C4s using conventional underfill. By measuring the two die stack theta-jc (chip center sensor to lid thermal resistance) and using an ANSYS conduction model of the package, it was possible to extract the TIM thermal resistance. Cross sections revealed roughly equivalent bond lines for the 2-D and 3-D stack test vehicles. Therefore, assuming the same TIM thermal resistance as the 2-D package, and using the measured 3-D stack theta-jc, it was possible to extract R_{dd} for the 3-D stack using the package model. The results revealed $R_{dd} = \sim$95 C mm^2/W. Table II summarizes the measurements of theta-jc and model extraction of R_{dd}. Since Figs. 8–11 assumed 14-μm tall micro-C4s, and most of the resistance would be the micro-C4 layer, a linear extrapolation of the 70-μm tall measured results to 14 μm would result in $R_{dd} \sim$ 19 C mm^2/W. This is certainly consistent with the range of values shown in Figs. 8 and 9, for no TSV (or very large pitch), with underfill and dielectric conductivities in the ranges indicated in the figures. A direct validation of the unit cell model used for Figs. 8–11 is not possible due to the unknown underfill and C4 thermal conductivities in the test vehicle form factor. As stated previously, the purpose of the measurement comparison was more to serve as a sanity check.

V. INTERFACIAL THERMAL RESISTANCE CONTRIBUTION

Implicit in the previous sections was that the interfacial thermal resistance between the material layers was negligibly small. Significant work has been conducted to analyze the thermal resistance at the interface of dissimilar materials. Nan [6] looked at SiC composites with whiskers and measured total effective thermal resistance, from which the individual resistance components were back-calculated. The interfacial thermal resistance component was found to be roughly 0.001 to 0.1 C mm^2/W. Molecular-dynamics-based studies include those of Yang [7], who used a coupled molecular dynamics/FEM to model the interfacial and continuum characteristics at an interface. Wang [8] used the diffuse mismatch model (DMM) to look at 1250 different material interfaces. The results ranged from 0.001 to 0.1 C mm^2/W for most cases. The thermal resistances correlated with the ratios of average sound velocities within the materials. Fig. 13 plots the interfacial thermal resistances as a function of the ratio of average sound velocities. It must be noted that the DMM is a rough approximation and in fact not valid for interfaces between very similar materials.

We attempted to use the relationship developed by Wang to estimate the interface thermal resistance of typical BEOL layer material pairs. The results are shown in Fig. 14. The left axis shows the ratio of sound velocities for the material pairs, and the right axis shows the interface thermal resistance (*Rint*) using the sound velocity ratio relationship. The sound velocities

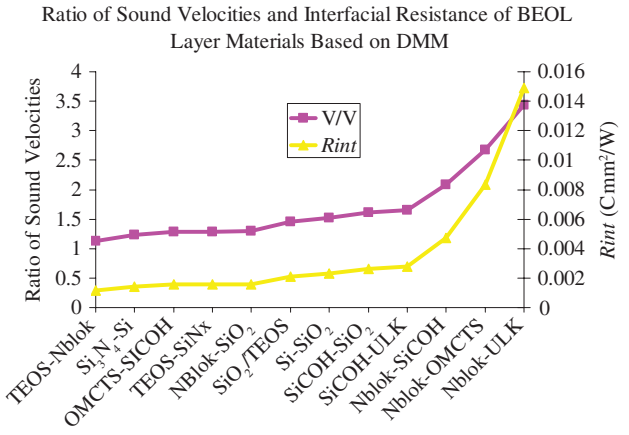

Fig. 14. Ratio of sound velocities (left axis) and interface thermal resistance (right axis) for common BEOL layer material pairs estimated using the *Rint*-to-sound velocity ratio relationship of Wang [8].

TABLE III
NUMBER OF INTERFACES AND INTERFACE THERMAL RESISTANCES PER INTERFACE FOR A TYPICAL 90-nm BEOL STACK

Interfaces	# Interfs.	*Rint* per interface (C mm^2/W)
TEOS-Nblok	6	0.001156
OMCTS-SICOH	1	0.001563
TEOS-SiN*x*	1	0.001569
NBlok-SiO_2	4	0.001592
SiO_2/TEOS	1	0.002089
SiCOH-SiO_2	4	0.00261
SiCOH-ULK	7	0.002783
Nblok-SiCOH	1	0.004715
Nblok-OMCTS	1	0.008365
Nblok-ULK	7	0.014891
Total thermal resistance		~0.17

were calculated as follows:

$$v_{avg} = \frac{v_L + 2v_T}{3}$$
$$v_L = \sqrt{\frac{C_{11}}{\rho}}, \quad v_T = \sqrt{\frac{C_{44}}{\rho}} \tag{3}$$

where C_{11}, C_{44}, and ρ are the Young's modulus, shear modulus, and density of the material, respectively. Modulus and densities of most of the BEOL materials were measured directly or estimated from representative material compositions at IBM. (Different variations of some of the materials exist, but properties are in general similar among families.) Generic properties were used for Si and SiO_2 as obtained from the literature. As can be observed from Fig. 13, the uncertainty can be as high as an order of magnitude for the lower sound velocity ratios.

Table III shows the numbers of such interfaces in a typical IBM BEOL layer stack and the value of the total interfacial thermal resistance contribution of a stack in a sub-90-nm generation microelectronic technology. The number of interfaces and estimated thermal resistance per interface are shown. As can be seen, the total theoretical interfacial contribution (~0.17 C mm^2/W) is quite small relative to the thermal resistance numbers discussed in the previous sections.

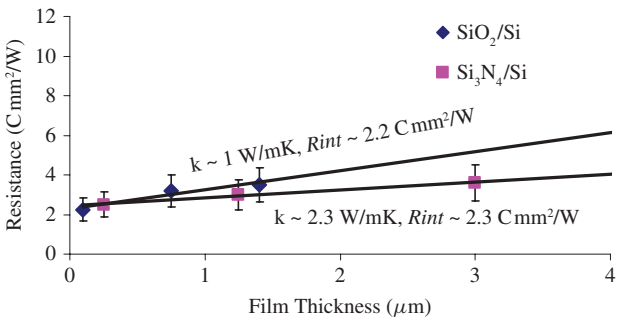

Fig. 15. Interfacial thermal resistances extrapolated from resistance versus film thickness for SiO_2 and Si_3N_4 on Si. Data from [9].

TABLE IV
INTERFACE THERMAL RESISTANCE BETWEEN METAL AND SiO_2 CALCULATED USING TWO FLUID MODEL AND MEASUREMENTS. DATA FROM [10]

Metal–SiO_2 interface	Two-fluid model C mm^2/W	Measurement C mm^2/W
Cr	7.1×10^{-4}	2.4×10^{-2}
Ti	3.9×10^{-4}	3.4×10^{-2}
Al	1.3×10^{-3}	3.5×10^{-2}
Ni	8.1×10^{-4}	3.5×10^{-2}
Pt	1.6×10^{-3}	3.8×10^{-2}

Another method to estimate the interfacial thermal resistance is to extrapolate the resistance versus film thickness measurements as was done by Lambropoulos [9], who summarized the extensive work of thermal conductivity measurements of thin films. Fig. 15 shows the thermal conductivity of oxide films as a function of thickness, summarized from other sources by Lambropoulos [9]. The interfacial thermal resistances are quite large for SiO_2 to Si and Si_3N_4 to Si (>2 C mm^2/W). These values are more than two orders of magnitude larger than those shown in Fig. 14 based on the DMM methodology.

The metal dielectric interface was analyzed by Chien [10], who used a sandwich structure of different metal layers between two dielectric oxide layers and compared measured thermal resistance to phonon/electron nonequilibrium based theoretical results. The interfacial thermal resistances extracted were about an order of magnitude higher than those predicted by the two-fluid model

$$R_{SiO_2-m} = \left(\frac{\delta}{k_e + k_p}\right)\left(\frac{k_e}{k_p}\right)\left[\frac{e^{\frac{L}{\delta}} - 1}{e^{\frac{L}{\delta}} + 1}\right] \tag{4}$$

where L is thickness of metal layer

$$\delta = \sqrt{\frac{k_e k_p}{G(k_e + k_p)}}$$

G is the electron–phonon coupling factor;
k_e is related by Wiedemann–Franz law;
$k_p = Cvl/3$;
C *is the* phonon specific heat from Dulogn–Petit law;
l is the phonon mean free path assumed to be 2X lattice constant;
v is the sound velocity.

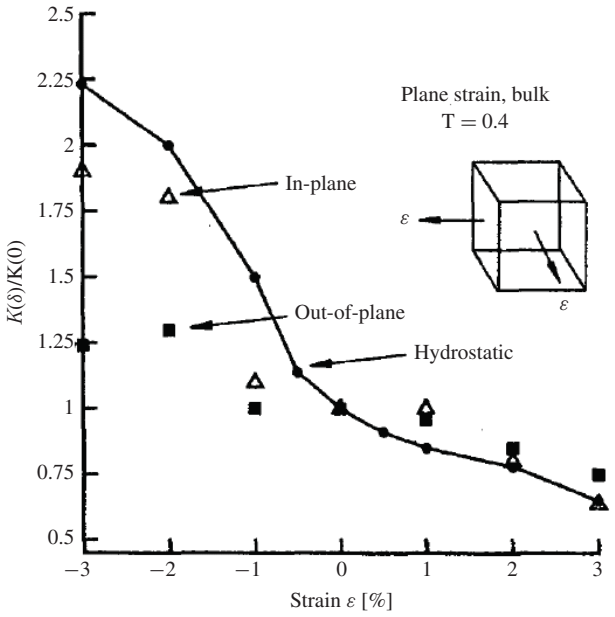

Fig. 16. Effect of strain on thermal conductivity of a Lennard–Jones solid. Both hydrostatic (lines) and in-plane strain components are shown. Reprinted with permission from [12].

The modeled and measured results are summarized in the Table IV.

Chien explained the model/measurement discrepancies as due to imperfections at the interfaces, such as voiding. Prasher [11] attempted to relate the higher interface thermal resistance due to imperfections to the materials' adhesion energy.

In summary, the review of prior work on the interfacial thermal resistance between dissimilar materials reveals significant disparity between theoretical and experimental results, which can only be explained by the imperfections at the interface. The comparison of R_{dd} extracted from the 3-D stack test vehicle suggests that the imperfections in actual BEOL layer stacks might not be as alarmingly high as the measurements by Lambropoulos and Chien might suggest.

VI. Strain Effect

Another factor seldom considered in calculation of the overall thermal resistance is the impact of strain. Picu [12] used a monatomic Lennard-Jones solid assumption and a molecular dynamics simulation to calculate the thermal conductivity of the solid under plane strain and plane stress conditions. He found that plane strain condition affected thermal conductivity, but plane stress had a negligible impact. Hydrostatic strain had the largest impact. The results of the plane strain and hydrostatic strain are shown in Fig. 16. The effects are due to change of phonon group velocities and mean free paths resulting from the strains. The plane strain condition actually makes the thermal conductivity anisotropic. Assuming less than 2% strains, and linearizing their findings, one can conclude that the strained to unstrained thermal conductivity ratio is

$$\frac{k}{k_o} \simeq [1 - 0.21(\%\varepsilon)] \tag{5}$$

which is in an averaged isotropic value (between the hydrostatic and plane strain conditions).

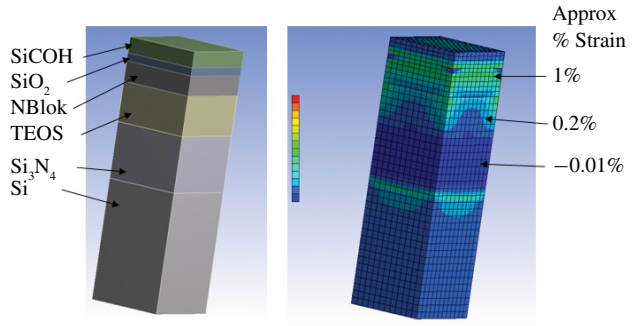

Fig. 17. ANSYS model of BEOL layer material stack on Si and resulting max. principal strains due only to thermal loading due to the deposition processes. Assumed coefficients of thermal expansion (CTEs) (ppm/°C) NBlok = 3, Si = 2.6, SiCOH = 12, SiN = 3, SiO_2 = 12, and TEOS = 0.6.

Bhowmick [13] explained the strain dependence of thermal conductivity as manifested in the group velocity (speed of sound) and relaxation time. However, the only strain condition analyzed was hydrostatic strain. In this paper, the phonon frequency was related to strains and, compared with a molecular dynamics simulation, showed good comparison. The relaxation time was related to temperature and strain as follows:

$$\tau \sim \frac{1}{T}\varepsilon^{-\gamma} \tag{6}$$

where γ is a material constant. The relationship of group velocity to strain was approximately

$$\frac{k}{k_o} \simeq [1 - 0.20(\%\varepsilon)] \tag{7}$$

which is fairly close to that extracted from Picu (5). Using the above relationship, we tried to find the impact of strain on the thermal conductivities of typical BEOL layer materials. As a test case, the strains developed in a six-layer stack shown in Fig. 17, arising purely from the CTE mismatch and thermal loading from deposition temperatures, were analyzed using ANSYS. The average CTE values measured at IBM were used for most dielectric materials, and from the literature for SiO_2 and Si. In an actual BEOL structure, the strain fields would be much more complicated due to the metal lines, vias, and package influences. It is obvious from Fig. 17 that there would be some layers in tension and others in compression. For 1% tensile strain in the SiO_2 layer, as shown in Fig. 17, the value of k/k_0 would be ~0.8. However, the majority of the layers are either in compression or unstrained. It is therefore argued that, while design-dependent, the net effect of the strain on thermal resistance of the BEOL is likely to be negligible over a large area. However, localized regions could be affected.

VII. Summary and Conclusion

The primary objectives of this paper were to quantify the added thermal resistance (R_{dd}) due to the BEOL and micro-C4 layers for 3-D stacked packages and identify the major and minor contributions. R_{dd} values on the order of or larger than the total 2-D package thermal resistances for today's high-powered applications imply significant cooling challenges for

two or more die-layer stacks. The study revealed the micro-C4 interconnects are significantly impacted by the adjacent BEOL layer thermal resistance and could not be analyzed separately due to the spreading and interaction effects. Analysis of TSVs revealed that only for pitches below $\sim$150 μm and for TSVs directly aligned with micro-C4s and which penetrate a significant portion of the BEOL layers would there be significant impact on R_{dd}. The interfacial thermal resistance of BEOL materials was evaluated based on the work of others, and revealed vastly different conclusions for theoretical and experimental analysis. The disparity is believed to be due to imperfections at the interfaces. The impact of strain on the thermal resistance of BEOL layers was analyzed and suggested to have a difficult-to-quantify but negligibly small impact over large areas, and possibly more of a concern for local regions.

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Jamil Wakil received the B.S. degree in mechanical engineering from Texas A&M University, College Station, the B.S. degree in electrical engineering from the University of Texas, Dallas, and the M.S. and Ph.D. degrees in mechanical engineering from the University of Texas, Austin.

He joined the IBM Microelectronics Packaging Group, New York, NY, in 1999, where he spent 10 years on first-level thermal development of organic packages and 3-D stack packages. He is currently working on data center thermal development for IBM systems, focusing on water cooling and energy efficiency. He has been awarded eight patents and has published several refereed research papers.

Evan G. Colgan (SM'85) received the B.S. degree in applied physics from California Institute of Technology, Pasadena, in 1982, and the Ph.D. degree in materials science from Cornell University, Ithaca, NY, in 1987.

He joined IBM, New York, NY, in 1987, and worked on silicides, selective chemical vapor deposition-W, diffusion barriers, and both Cu- and Al-based chip wiring. He moved to manage the Thin Film Transistor Processing Department, IBM Research Division, New York, in 1995, as a Research Staff Member, and subsequently worked on a number of display-related projects. He joined the packaging area in 2001 and has worked on optical packaging, high-performance liquid cooling, super computer packaging, and 3-D chip packaging. He has published over 100 technical papers and has been awarded 103 U.S. patents.

Dr. Colgan is a member of the American Physical Society and the Market Research.

Shaochen Chen is a Professor in the Nanoengineering Department at the University of California, San Diego (UCSD). He is also a faculty member of the Institute of Engineering in Medicine, UCSD. Before joining UCSD, he had been a Professor and a Pearlie D. Henderson Centennial Endowed Faculty Fellow in engineering in the Mechanical Engineering Department, University of Texas, Austin. His current research interests include biomaterials and biofabrication, nano-regenerative medicine, laser nanomanufacturing, nanophotonics, plasmonics and metamaterials, and bio- and nano-mechanics.

Dr. Chen served as the Program Director for the Nanomanufacturing Program in the National Science Foundation (NSF) from 2008 to 2010, where he directed the frontiers of nanomanufacturing research at NSF and managed 150 active grants of the program. In 2001, he received the CAREER Award from NSF for cutting-edge research in laser nano-scale processing of biodegradable polymers. In 2004, he received the Young Investigator Award from the Office of Naval Research for his work on nanocomposites with unique optical, thermal, and chemical properties. As an active member in his professional community, he was elected as a Fellow of the American Society of Mechanical Engineers in 2007, the International Society for Optical Engineering in 2008, and the American Association for the Advancement of Science in 2011. Currently, he serves as the Associate Editor for *Journal of Biomedical Nanotechnology*. He is also on the Editorial Board of several journals including *Nanomedicine, Biofabrication, The Open Materials Science Journal, Journal of Nanoengineering and Nanomanufacturing*, and *Journal of Nano Energy and Power Research*.