

Jamil A. Wakil

Advisory Engineer
IBM Corporation,
11400 Burnet Rd.,
Austin, TX 78758
email: jwakil@us.ibm.com

Patrick W. Dehaven

Senior Engineer
IBM Corporation,
2070 Rt. 52,
Hopewell Junction, NY 12533
email: dehaven@us.ibm.com

Nancy R. Klymko

Senior Technical Staff Member
IBM Corporation,
2070 Rt. 52,
Hopewell Junction, NY 12533
email: klymko@us.ibm.com

Shaochen Chen

Professor
University of California San Diego,
9500 Gilman Drive #0448,
La Jolla, CA 92093
email: shc064@ucsd.edu

Thermo-Mechanical Response of Thru-Silicon Vias Under Local Thermal Transients Using Experimentally Validated Finite Element Models

Significant research has focused on the reliability of through-silicon-vias (TSVs) under conventional uniform thermal loading conditions such as accelerated thermal cycling (0–100 °C) or deep thermal cycling (–40–125 °C). This study analyzes the thermomechanical behavior of TSVs in 3D packages undergoing rapid local temperature fluctuations, as would be experienced in actual operation. A global/local finite element model is used to analyze the TSV behavior at various distances from the thermal fluctuation site. Transient thermal measurements, warpage and in-plane deformation measurements, as well as micro-Raman spectroscopy measurements are used to validate the model. The results reveal that the short term local temperature transients have minimal impact on the TSV stress state regardless of TSV location, implying that global package-induced stresses dominate. [DOI: 10.1115/1.4004656]

Introduction

3D packaging has spurred significant research into manufacturability and reliability of thru-silicon vias (TSVs) [1–6]. Stress and reliability studies primarily focus on the stresses induced due to the coefficient of thermal expansion (CTE) mismatch between the TSV material and silicon, with fewer addressing package induced stresses in uniform temperature cycling tests [7–12]. Even fewer have examined TSV mechanical behavior under nonuniform temperature or highly transient and localized thermal loadings [13,14]. The goal of this study is to analyze the stresses under rapid local temperature transients experienced in application conditions, including the influence of package stresses. The modeling methodology and experimental validation with thermal, digital image correlation (DIC), and micro-Raman spectroscopy measurements will be described. Results from the finite element analysis will reveal the impact of local temperature transients on the stress state of a TSV near and far from the localized hotspots.

Model Description

Figure 1 shows the ANSYS™ finite element models used for calculating the temperature and stress fields. A global/local modeling scheme was used in which the displacement boundary conditions for the local model were obtained from the coarser quarter symmetry global model.

Figure 2 shows the grid and time-step sensitivity analysis. The solid lines represent maximum die temperature for the steady state thermal analysis, and laminate warpage for the mechanical analysis as a function of the number of total elements in the model. Grid smoothing and expansion parameters were kept constant. The dotted line (referencing the right and upper axis) shows the maximum die temperature as a function of time step one second after a power transient. Roughly 110,000 nodes and 60,000 elements were chosen as optimal for the global model. It was found that a minimum time step

of 0.01 s was sufficient to capture the max thermal transients to be studied. A similar analysis was used to find the optimal grid for the local mechanical model, which resulted in roughly 200,000 nodes and 130,000 elements being chosen, with finer mesh in the regions of interest (TSVs). The local model was more sensitive to mesh due to interpolation of boundary conditions from the global model at surface nodes. Both tetrahedral and brick elements were used to balance grid size and simplicity of mesh generation. ANSYS is able to connect different types of elements as long as degrees of freedom are consistent. The global/local modeling scheme made plastic, incremental analysis prohibitive without custom coding. Instead, great care was taken to calibrate the simplified conduction, linear elastic model with experimental data. Significant attention is therefore given to describe the model validation process in subsequent sections.

The finite element model solves the fundamental equations for thermo-elasticity. For static analysis and isotropic materials, the fundamental equations in index notation are [15]:

Stress–strain relation

$$\varepsilon_{ij} = \frac{(1 + \nu)\sigma_{ij}}{E} - \frac{\nu\sigma_{kk}}{E}\delta_{ij} + \alpha(T - T_0)\delta_{ij} \quad (1)$$

The strain–displacement relation

$$\varepsilon_{ij} = \frac{1}{2} \left(\frac{\partial(u_i)}{\partial x_j} + \frac{\partial(u_j)}{\partial x_i} \right) \quad (2)$$

Heat conduction equation

$$\frac{\partial}{\partial x_i} \left(\frac{\partial T}{\partial x_i} \right) + \frac{\dot{q}}{k} = \frac{1}{\tilde{\alpha}} \frac{\partial T}{\partial t} + T_0 C \frac{\partial \varepsilon_{ii}}{\partial t} \quad (3)$$

Equilibrium

$$\sigma_{ij,j} + F_i = 0 \quad (4)$$

where: ε = total strain, σ = stress, $\delta = 0$ if $i \neq j$, or 1 if $i = j$, α = coefficient of thermal expansion (CTE), $\tilde{\alpha}$ = thermal diffusivity,

Contributed by the Electronic and Photonic Packaging Division of ASME for publication in the JOURNAL OF ELECTRONIC PACKAGING. Manuscript received March 31, 2010; final manuscript received June 6, 2011; published online September 14, 2011. Assoc. Editor: Kikuo Kishimoto.

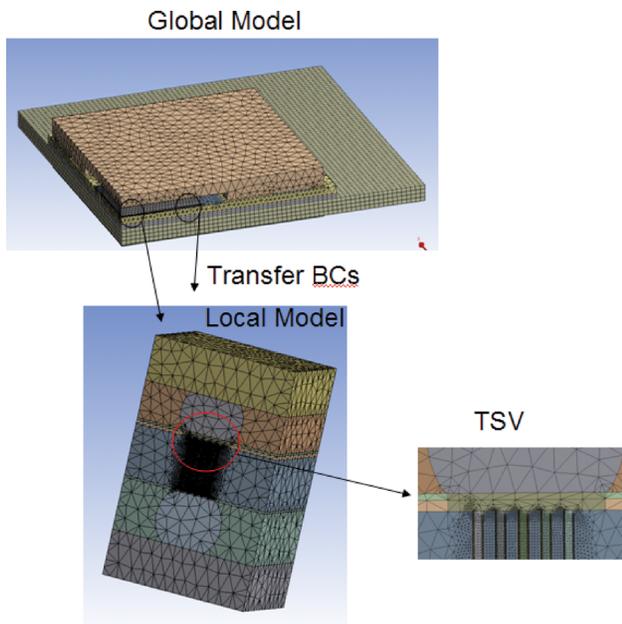


Fig. 1 Package level and TSV (local) level validation ANSYS models

$T = T(x,y,z)$ = temperature field, $T_0 = T_0(x,y,z)$ = reference temperature field, ν = Poisson ratio, E = Young's Modulus, u = displacement, k = thermal conductivity, q = heat generation, C = material constant, F = force

The last term in Eq. (3) is the temperature-strain coupling term (where C is a constant related to the material elastic constants and thermal conductivity). The coupling term represents viscous energy dissipation and is typically neglected if the strain/deformation rate is sufficiently small (less than speed of sound in the material). This assumption will be used, and its validity addressed when analyzing the final results. The temperature field can then be solved independently. This also allows use of the global/local modeling technique. The thermoelasticity problem then involves finding sixteen unknowns: σ_{ij} , ϵ_{ij} , u_i , T , using Eqs. (1-4) which together give sixteen relations.

Validation Test Vehicles for Global Model

The first task was to properly calibrate the linear thermal and mechanical global model with measurements from 2D and 3D stacked test vehicles. (The TSV micromodel validation will be described

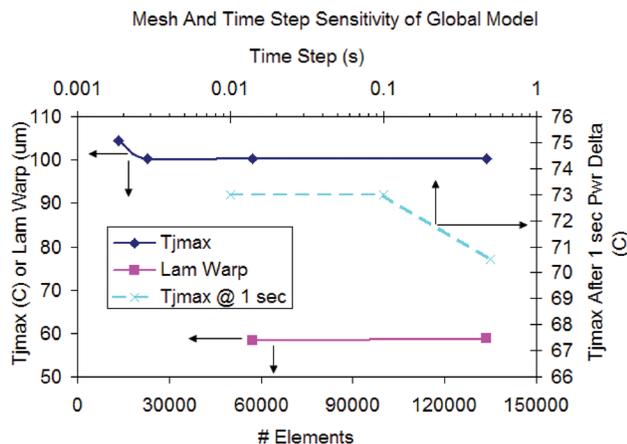


Fig. 2 Mesh sensitivity analysis for the global package model. Tjmax and laminate warpage as a function of number of elements (left and bottom axis) and Tjmax after 1 s power delta as a function of time step (right and upper axis)

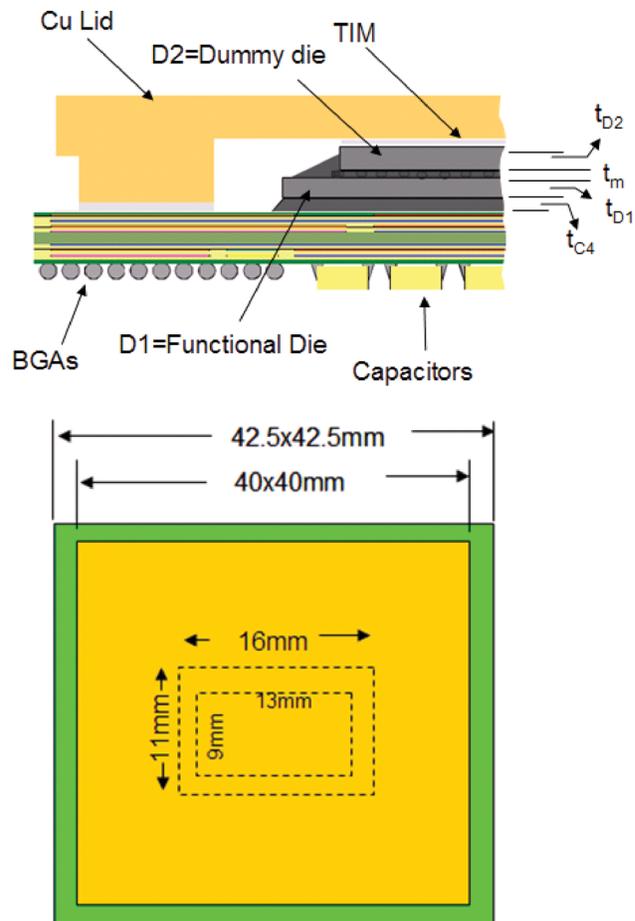


Fig. 3 Schematic showing the module components and lateral dimensions

subsequently). Figure 3 shows the dimensions and components of 3D stack test vehicles used for the global thermal/mechanical validation. The test vehicles contained a functional thermal test die on the lower layer, and a nonfunctional dummy die adhered on top using conventional underfill epoxy. The top schematic shows only half the module and shows the bottom die (D1), top die (D2), die-die microC4 (m), and C4 thickness designations. Also highlighted are the Cu lid, thermal interface material (TIM), BGA's and capacitors. (The capacitors served no purpose for this study). The thickness values are summarized in Table 1. In addition, standard 2D packages (not shown) with all similar components except one die layer were used for comparison. Test vehicles with and without lid and card were used for establishing different component properties, as will be discussed later. Figure 4 shows a sample cross section of one of the 3D stack test vehicles.

Global Thermal Model Validation

The functional test die contained heaters for applying uniform heat on the chip active surface, and temperature sensing resistors

Table 1 Average thicknesses of C4, microC4 (t_m), bottom die (t_{D1}) and top die (t_{D2}), and thermal interface material (TIM)

	3D Stack	2D
t_{TIM}	32 (μm)	28 (μm)
t_{D1}	766	770
t_{D2}	758	NA
t_m	68	NA
t_{C4}	54	58

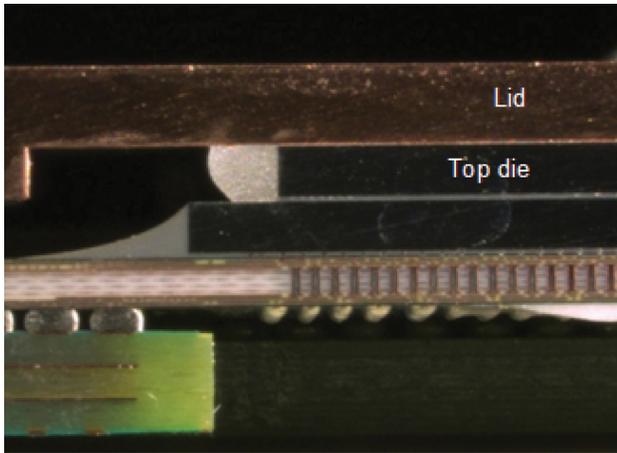


Fig. 4 Cross section of the 3D stack used for global model validation

at various locations on the die to measure temperature. The temperature sensors were calibrated in an oven using a multiplexed constant current source and voltage meter. Testing was conducted on a water cooled cold plate as shown in Fig. 5. This ensured simple boundary conditions to simulate in the finite element model and would be similar to the application boundary conditions of high powered processors.

The thermal validation strategy was as follows:

- (1) 2D chip-to-lid steady-state thermal resistance measurements to determine TIM resistance.
- (2) 3D stack pkg steady-state chip-to-lid resistance measurements to determine die-die interface resistance using TIM values obtained from step 1 and bondline information from cross sections.
- (3) Lidded cold plate transient measurements to determine appropriate conductivities and thermal diffusivities for rest of components.

For all materials or composites, initial properties based on previous in-house measurements or vendor data were used. Those thermal properties (conductivity, density, and specific heats) without prior direct measurements were then adjusted to match the measurement results. These primarily included the BGA/air layer and the laminate carrier composite properties. The heat transfer coefficients were determined from steady state measurements since the cold plate flow rates were kept constant for all runs. Typical values ranged from 4500 to 5500 W/m²K applied to the lid top surface (representing the cold plate and oil interface to the cold plate), all other vertical surfaces were fixed at 30 W/m²K and the horizontal surfaces at 10 W/m²K.

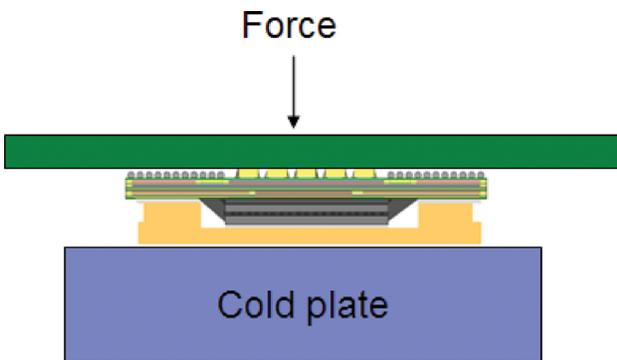


Fig. 5 Testing on a cold plate

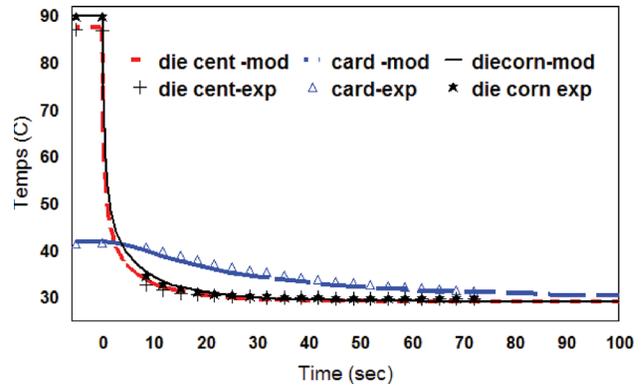


Fig. 6 Model/Experiment comparison for stack package with 9 × 13 mm die on 11 × 16 mm, showing die center, card, and die corner temperatures. Uncertainty of temperature measurements is less than ±1 °C.

Figure 6 shows the model/experiment comparison for the standard 3D stack package with a 9 × 13 mm die on an 11 × 16 mm, showing temperature comparisons as the powered package (60 W) is shut off after achieving steady state and cooled down to the cold plate temperature of 30° C. The lines are modeled results, and the dots are the corresponding experimental data. The three temperature points are the die center (die cent), card top (card), and die corner (die corn). As can be seen the model-to-experiment correlation is excellent. Both the steady state (time < 0) and transient temperatures are within ~10% agreement at worst. The measurement uncertainty is ~±1 °C.

The final thermal properties determined from the thermal validation are shown in Table 2.

Global Mechanical Validation

Transient analysis which required global and local modeling made the use of plastic incremental/path dependent modeling prohibitive. Consequently, considerable effort was made to properly validate and calibrate the linear elastic models. With the models accurately predicting behavior under test conditions, the subsequent results and conclusions from linear models could be accepted with more confidence.

A digital image correlation system by GOM mbH was used to validate the mechanical properties of the global model. The technique is based on collecting digital images, assigning coordinates to the image pixel groups (facets), and tracking the pixels to calculate deformation. Each facet determines a calculation point in the image. The system software essentially runs a minimization routine for the difference between a point and its surroundings at its old coordinates versus new coordinates. Rigid body motions can be subtracted out. For 3D warpage measurements, two cameras are required to calculate facet locations in three-dimensional

Table 2 Thermal material properties resulting from validation experiments

	Thermal conductivity (W/mK)	Specific heat (J/kgK)	Density (kg/m ³)
C4/Underfill	1	1000	1700
Card	3xy, 1z	2000	1700
Lid	380	385	8300
Laminate	75xy, 6z	1600	1700
Die-Die interface	1	1000	1700
Silicon	130	700	2330
BGA layer	0.34xy, 8z	134	5500
Lid adhesive	1	500	2000
Thermal interface (TIM)	2.5	500	2000

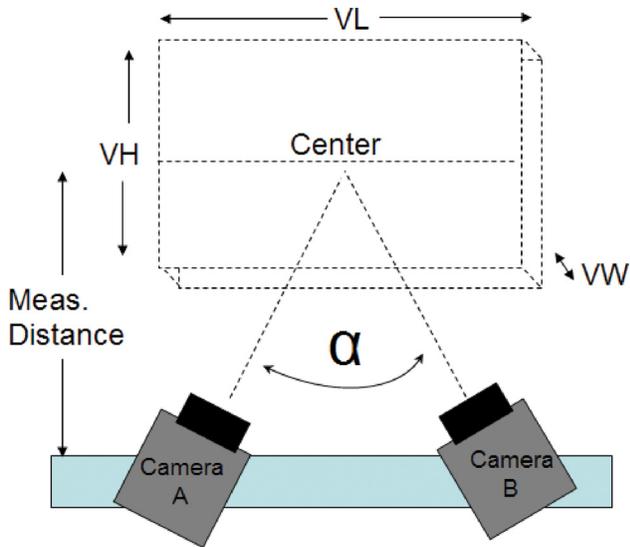


Fig. 7 Camera setup and measurement volume for 3D DIC measurement

space. The setup and measuring volume are shown in Fig. 7. The measurement accuracy is based on the necessary measurement volume. For the measurements made, out-of-plane accuracy was approximately $\pm 5 \mu\text{m}$, and in-plane approximately $\pm 2 \mu\text{m}$.

A systematic approach was used wherein samples ranging from bare-die-on-laminate to fully assembled modules-on-card were used to fix the properties for various components of the package. First, a bare die flip chip module was used to determine the laminate and underfill/C4 layer properties. Next a two die stack with-

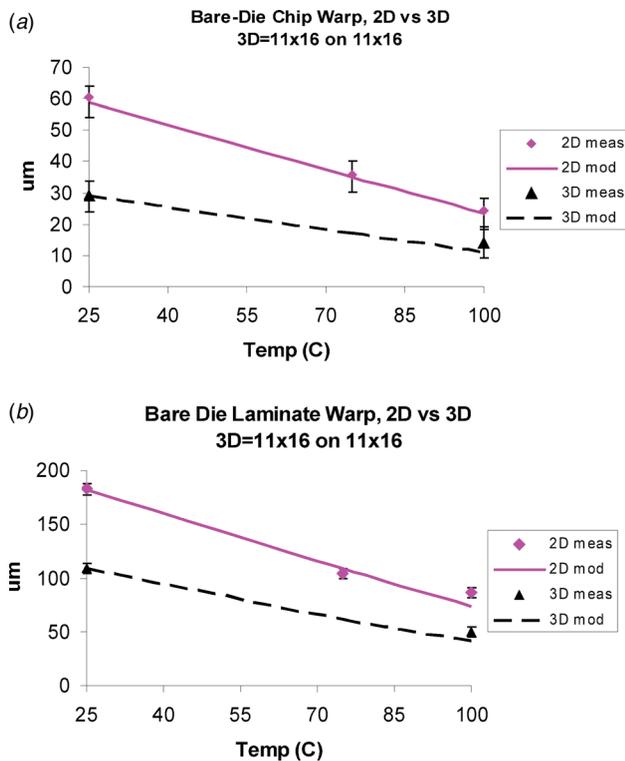


Fig. 8 Lidless chip (a) and laminate backside (b) warpages as function of temperature, measured and modeled, for bare die modules without card. Uncertainty of warpage measurements is estimated to be $\pm 5 \mu\text{m}$.

out lid or card was used to fix the die-to-die interface properties, and so on.

Figure 8 shows the lidless chip (a) and laminate bottom (b) warpage measurements (dots) as a function of temperature, and comparison with model (lines). The figure shows the conventional 2D module as well as an 11×16 on 11×16 mm die stack. As can be seen, the model and measurements are in close agreement.

Figure 9 shows the X and Y field deformations from 150°C to room temperature for the 9×13 mm on 11×16 mm stack package, with lid and card. The result along the center of the lid and laminate on the central cross section are shown. Although the X-field agreement with model is excellent, the Y-field has larger disagreement. This was a consistent trend with all lidded samples and believed to be due to nonflatness of the lid and nonidealities in the lid attach manufacturing process. Measurements of warpage and in-plane deformation for nonlidded samples (i.e., Fig. 8) generally agreed quite well for both X and Y-field, implicating the lid-attach process. In general, this is not believed to affect the accuracy of the model for the purposes of this work. Table 3 shows the elastic mechanical properties resulting from the experimental validation.

TSV Micromodel Validation

The TSV micromodel was validated using micro Raman spectroscopy measurements on a 3D package containing a $75 \mu\text{m}$ interposer with Tungsten TSVs. The objectives of the measurements were to validate the micromodel used to analyze TSV stresses imparted by the package. The principle of μRaman spectroscopy is the interaction of photons from a laser source and lattice vibration (phonons) in a crystal. This photon-phonon interaction results in inelastic scattering, which shifts the frequency of the scattered light, resulting in a Raman-shifted

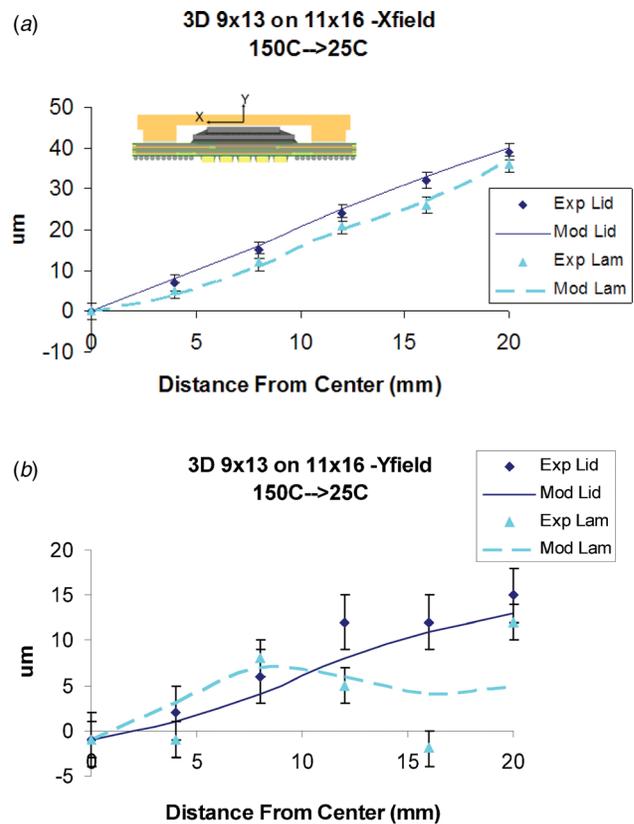


Fig. 9 X (along length of cross section) and Y (vertical) field deformations for $150^\circ\text{C} \rightarrow 25^\circ\text{C}$ for the 9×13 on 11×16 mm stack package. Uncertainty of in-plane deformation measurements is estimated to be $\pm 2 \mu\text{m}$.

Table 3 Calibrated mechanical properties resulting from validation experiments

	CTE (ppm/C)	Youngs Modulus (GPa)	Poisson ratio
C4/Underfill layer	27	12	0.4
Card	17	15	0.2
Lid	16	110	0.34
Laminate	16	25	0.3
Die-Die interface	27	12	0.4
Si	3.5	150	0.28
BGA layer	83	0.4	0.3
Lid Adhesive	240	0.001	0.45
TIM	250	0.00025	0.49

frequency. The Raman spectrum measures the scattered intensity vs. Raman shift in centimeter inverse [16].

When the material is strained, the scattered light frequency will shift. The relationship between the frequency shift and strain for

$$\begin{vmatrix} p\varepsilon_{11} + q(\varepsilon_{22} + \varepsilon_{33}) - \lambda & (p - q)\varepsilon_{12} & 2r\varepsilon_{13} \\ (p - q)\varepsilon_{12} & q\varepsilon_{11} + p\varepsilon_{22} + q\varepsilon_{33} - \lambda & 2r\varepsilon_{23} \\ 2r\varepsilon_{13} & 2r\varepsilon_{23} & p\varepsilon_{33} + q(\varepsilon_{11} + \varepsilon_{22}) - \lambda \end{vmatrix} = 0 \quad (5)$$

where ε_{ij} are strain tensor elements in the plane of cross section and p , q , and r are phonon material constants and $\lambda = \omega^2 - \omega_o^2$ are the eigenvalues. The shift of the Raman frequency from the unstrained value ω_o is given by $\Delta\omega = \frac{\lambda}{2\omega_o}$. Equation (5) results from relating the lowest order phonon modes to strain [17] and is only solvable for uniaxial or biaxial stress conditions. For a biaxial stress condition, as is assumed the case for an exposed cross sectional surface, the stress (Pa) to Raman shift (cm^{-1}) relationship for Si is given as [17]

$$-0.365 \times 10^{-9} \sigma_{xx} - 2.31 \times 10^{-9} \sigma_{yy} = \Delta\omega \quad (6)$$

Figure 10 shows a typical Raman spectrum for unstrained Si, showing the peak at $\sim 521/\text{cm}$. Compression shifts the peak higher, and tension shifts it lower. The laser plasma line is used for calibration.

Figure 11 shows the Raman spectroscopy measurement system used in this study. A HeCd laser was used as the light source, which is focused on the sample through a microscope. The scattered light is collected and analyzed using confocal optics and a single stage spectrograph CCD (charge-coupled device) detector.

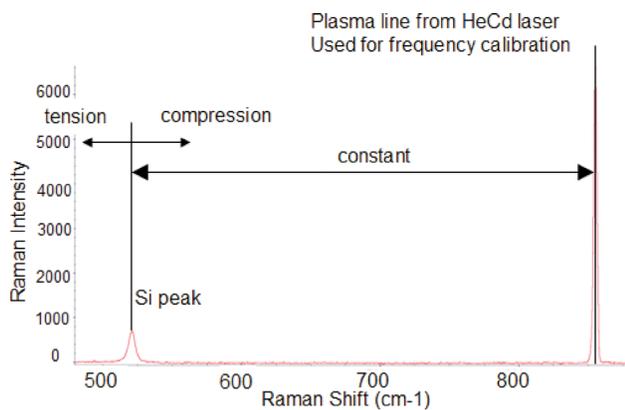


Fig. 10 Measured spectrum for unstrained Si

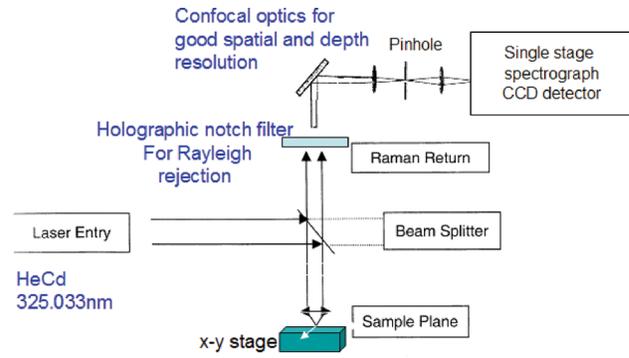


Fig. 11 Micro Raman measurement system

the cross sectional (110) surface of a silicon wafer can be found by solving the secular relationship [12]

The theoretical resolution limit for the HeCd laser with 325 nm excitation is ~ 440 nm in-plane at a depth of approximately 10 nm into Si.

Figure 12 shows an optical cross section image of the test vehicle containing the 75 μm interposer with TSVs and Fig. 13 shows a higher magnification image revealing the TSV bars in cross section and representative locations of μRaman measurements. A TSV was composed of seven bars, however, only five are visible in the cross section. This allowed better gauging of the location of the cross section normal to the image plane. The seven bars are approximately 3 μm wide, penetrate the thickness of the interposer from the lower to upper C4 pads and have varying lengths normal to the plane of cross section as depicted in the top view sketch of Fig. 13. There is approximately 1 μm of thermal oxide on each side of the bars. Figure 14 shows μRaman shift data in the silicon between two TSV bars near the top of the interposer at the edge of the chip

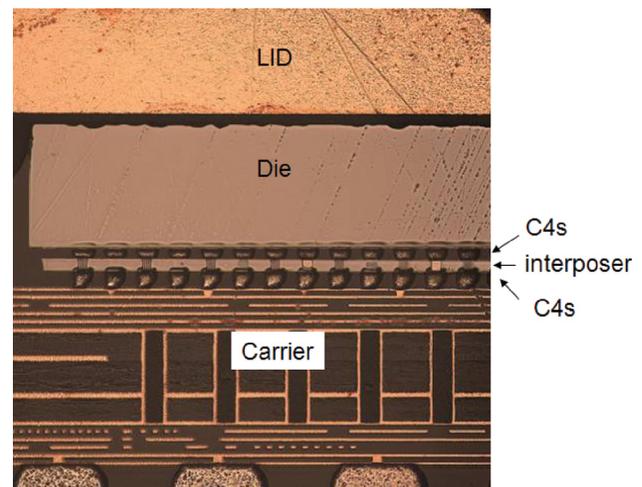


Fig. 12 Package cross section showing used for μRaman measurements

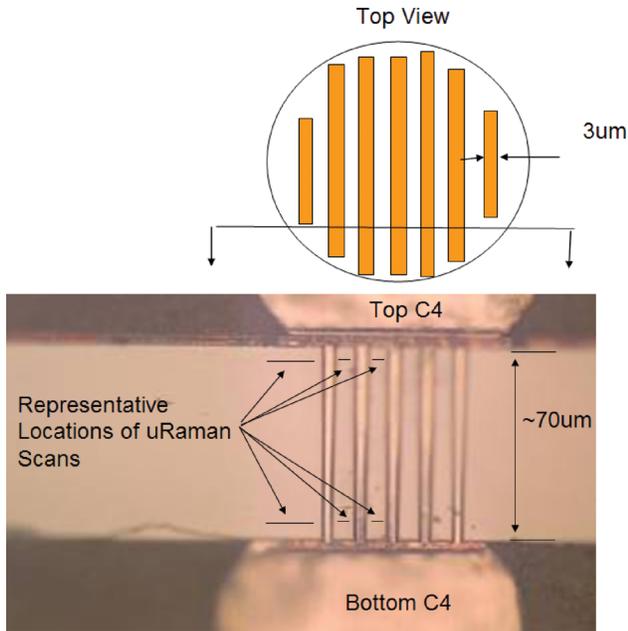


Fig. 13 High mag picture showing a W TSV bar grouping and locations of μ Raman measurements

Figure 15 shows a comparison of the modeled and measured data after validation. The lines are model results of top and bottom locations in a group of TSV bars at the center as well as edge of chip. The dots represent the corresponding measurement results.

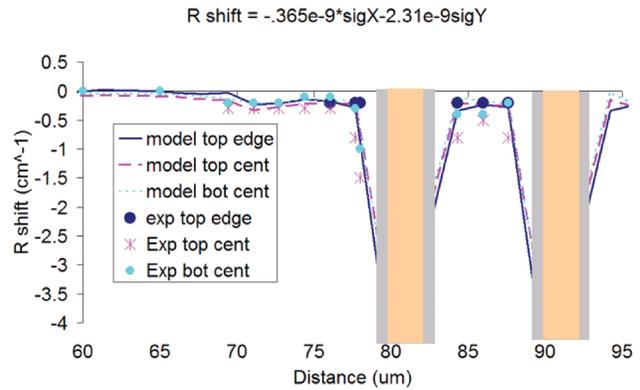


Fig. 15 Model (lines) and measurement (dots) comparison of μ Raman shift surrounding two leftmost visible TSV bars. The TSV bars are superimposed on the graph, including the $1 \mu\text{m}$ of oxide on each side. Measurement uncertainty is estimated to be $\pm 0.2 \text{ cm}^{-1}$.

Based on repeatability measurements, the uncertainty in the measured values is approximately $\pm 0.2 \text{ cm}^{-1}$. As can be seen, the model/measurement agreement is fairly good. The data within approximately $1 \mu\text{m}$ of the TSV was intentionally not plotted and deemed unreliable. This was due to the interdiffusion of oxide into the Si, resulting in no clear boundary between pure Si and oxide.

TSV Analysis

After validating the macro and micromodels, the package structure detailed in Table 4 was modeled to analyze the mechanical behavior of a TSV during a localized high-power transient event. The basic package structure was the same as that shown in Fig. 3, with the same lid design but some differences in the die and microC4 dimensions. The TSV structure and dimensions were the same as that shown in Fig. 13. The package was modeled on card with heat sink loading of 100 N and heat transfer coefficients to achieve die maximum temperatures of 85°C under uniform power of approximately 60 W.

Figure 16 shows the die center and package maximum temperature delta from steady state conditions as a function of time. The temperature increase at 1 s results when a $2 \times 2 \text{ mm}$ central region of the die is powered to 10X the power density of the rest of the die for 10 ms, followed by a complete power shut-down of the entire die. This could represent a scenario where a processor core undergoes a short period of high activity, followed by a turn-off of the entire processor. This represents the most severe situation in terms of thermal stress. The case of continuous die operation after the power spike is more benign. Only the first 3 s are shown to highlight the temperature spike which occurs at 1.0 s. The temperatures take approximately 200 s to reach steady state after power-off. Due to the higher heat transfer rate through the die and lid, the package laminate corners actually become the max package temperatures some time after power shutoff.

Three different cases were analyzed: Tungsten TSV at center of the die within the hotspot region, a Tungsten TSV at the edge of the chip (outside the hotspot), and a similar copper TSV

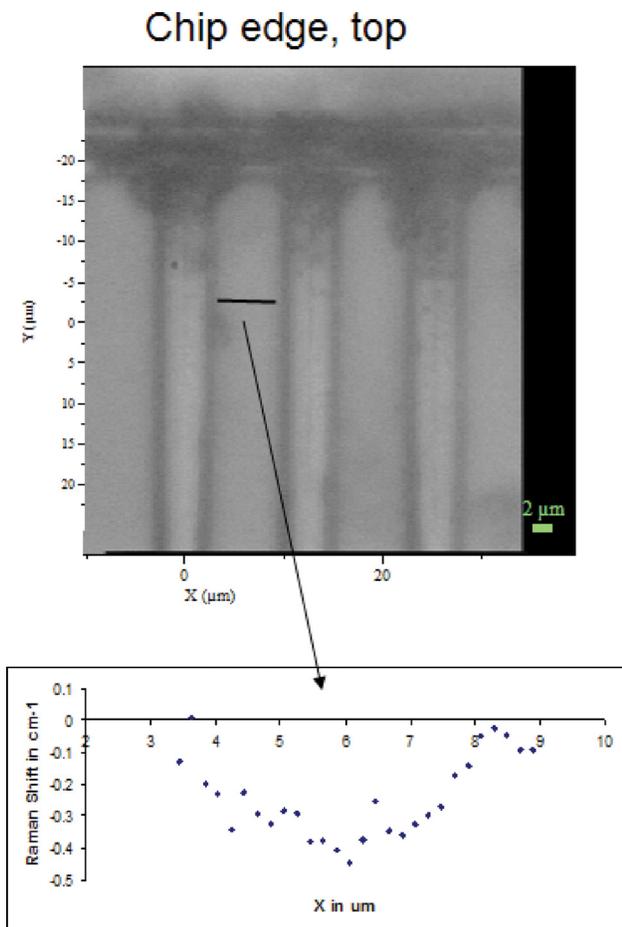


Fig. 14 Micro Raman measurement near TSV at top edge of interposer

Table 4 Dimensions of package used to analyze TSV behavior

	Dimensions
Package	$42.5 \times 42.5 \text{ mm}$
Top die	$11 \times 16 \times 0.785 \text{ mm}$
Bottom die	$11 \times 16 \times 0.070 \text{ mm}$
Micro-C4 height/diameter	20/40 μm

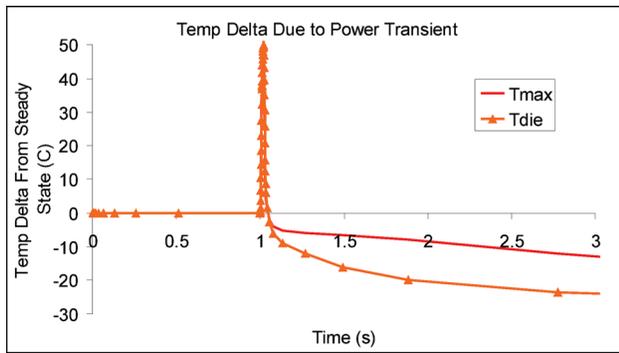


Fig. 16 Temperature profile resulting from hotspot power spike at 1 sec, used for TSV mechanical analysis, showing the first 3 s only.

instead of Tungsten at the chip edge. Figure 17 shows the normal Z-strain ratio (direction of TSV axis) for the three cases, as a function of time. The strain ratio is the ratio of actual strain to the strain at steady state operation. Figure 17(a) shows the total transient and Fig. 17(b) shows more detail of the time period of the hotspot power spike. As can be seen from Fig. 17(a), the Cu TSV at the edge of the chip has significantly more strain than the W TSV, due to its lower modulus. It is interesting to note that the center W TSV has slightly higher z-strain than at the edge. From Fig. 17(b), one can conclude that the temperature spike has

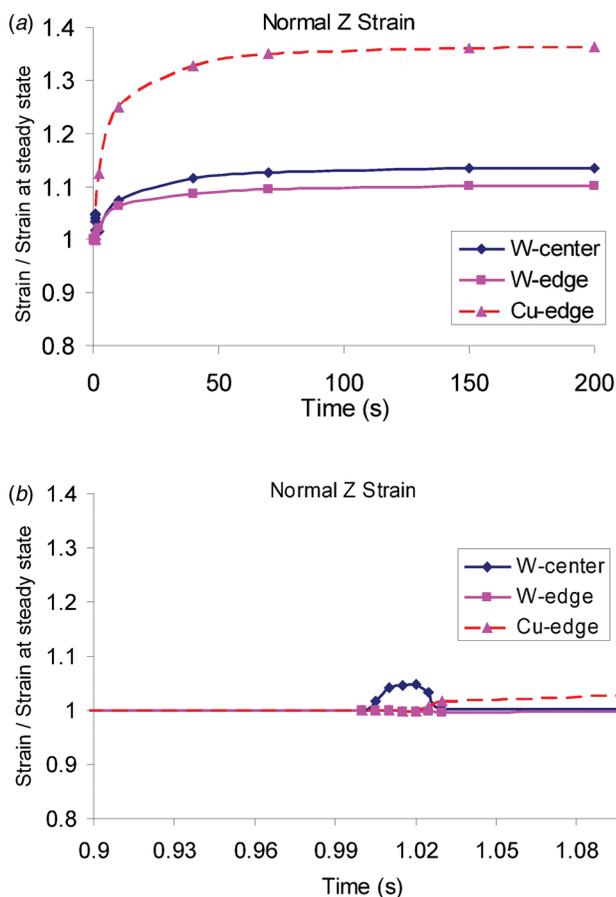


Fig. 17 Normal z strain ratio (parallel to TSV axis) as a function of time for the temperature profile of Fig. 16. (a) shows total time, (b) shows an expanded time scale near 1 s when the power spike occurs.

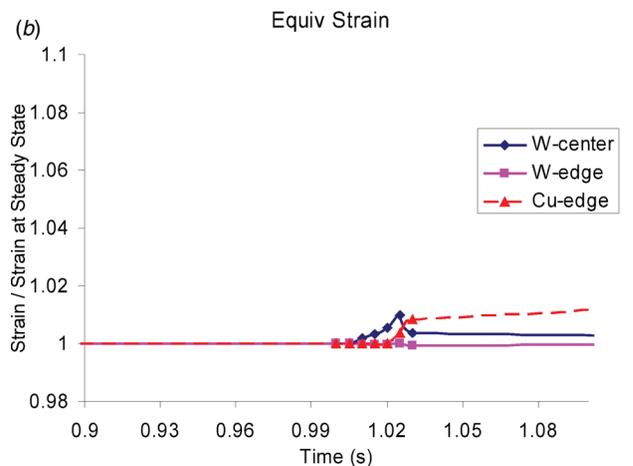
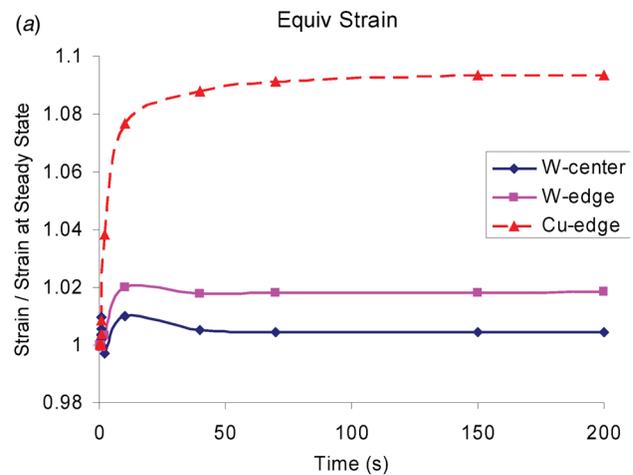


Fig. 18 Equivalent strain ratio as a function of time for the temperature profile of Fig. 16. (a) shows total time, (b) shows an expanded x-axis near 1s when the power spike occurs.

minimal effect on the strains, and in general could be ignored. It is also possible to conclude that the initial assumption of decoupling the thermal and mechanical analysis was valid, since the strain is negligible due to the short transient, and maximum strain rates are well below 10^{-2} /s. Stevenson [18] analyzed the stress-strain curve of Copper as a function of strain rate and concluded that below $\sim 10^3$ /s. The material was essentially insensitive to strain. Bose [19] did a similar analysis for Tungsten and found a very small strain rate sensitivity in the given temperature range. The temperature dependence of both Tungsten and Copper properties in the range of temperatures studied is also small. The use of constant, rate, and temperature independent properties therefore seems justified.

Figure 18 shows comparison of the equivalent strain ratio for the three different cases. The plot leads to similar conclusions as the normal strain plot: showing significantly higher strains for the lower modulus copper TSV. The equivalent strains are slightly lower at the center than the edge location. The results reveal that local power transients resulting in significant local temperature fluctuations have minimal impact on the strain within a TSV, regardless of location.

Summary and Conclusions

A global/local modeling scheme was used to analyze the mechanical behavior of TSVs under localized thermal transients. The global models were validated with thermal and mechanical

measurements using 3D stack test vehicles. The local TSV model was validated using μ Raman spectroscopy of the Silicon surrounding the TSV structures. The results revealed negligible impact of localized thermal transients on the TSV stress state, regardless of the location of the TSV in the die or proximity to the hotspot.

References

- [1] Newman, M. W., Muthukumar, S., Schuelein, M., Dambrauskas, T., Dunaway, P. A., Jordan, J. M., Kulkarni, S., Linde, C. D., Ophelm, T. A., Stingel, R. A., Worgag, W., Topic, L. A., and Swan, J. M., 2006, "Fabrication and Electrical Characterization of 3D Vertical Interconnects," Proceedings ECTC.
- [2] Ranganathan, N., Prasad, K., Balasubramanian, N., Qiaoer, Z., and Hwee, S. C., 2005, "High Aspect Ratio Through-Wafer Interconnect for Three Dimensional Integrated Circuits," Proceedings ECTC.
- [3] Hon, R., Lee, S. W. R., Zhang, S. X., and Wong, C. K., 2005, "Multi-stack Flip Chip 3D packaging with Copper Plated Through Silicon Vertical Interconnection," Proceedings ECTC.
- [4] Murrow, P., Black, B., Kobrinsky, M. J., Muthukumar, S., Nelson, D., Park, C., and Webb, C., 2007, "Design and Fabrication of 3D Microprocessors," Proceedings MRS Symposium, Vol. 970.
- [5] Bower, C. A., Malta, D., Temple, D., Robinson, J. E., Coffman, P. R., Skokan, M. R., and Welch, T. B., 2006, "High Density Vertical Interconnects for 3-D Integration of Silicon Integrated Circuits," Proceedings ECTC.
- [6] Takahashi, K., Taguchi, Y., Tomisaka, M., Yonemura, H., Hoshino, M., Ueno, M., Eqawa, Y., Nemoto, Y., Yamaji, Y., Terao, H., Umemoto, M., Kameyama, K., Suzuki, A., Okayama, Y., Yonezawa, T., and Kondo, K., 2004, "Process Integration of 3D Chip Stack with Vertical Interconnection", Proceedings ECTC.
- [7] Noritake, C., Limaye, P., Gonzalez, M., and Vandeveld, B., 2006, "Thermal Cycle Reliability of 3D Chip Stacked Package Using Pb-free Solder Bumps: Parameter Study by FEM Analysis," Proceedings EuroSimE Conference.
- [8] Hsieh, M. C., Hsu, Y., and Chang, C., 2006, "Thermal Stress Analysis of Cu/Low-k Interconnects in 3D-IC Structures," Proceedings IEEE Int. Microsystems, Packaging, and Assembly Conference.
- [9] Tanaka, N., Sato, T., Yamaji, Y., Morifuji, T., Umemoto, M., and Takahash, K., 2002, "Mechanical Effects of Copper Through-Vias in a 3D Die-Stacked Module," Proceedings ECTC.
- [10] Zhang, J., Bloomfield, M. O., Lu, J., Gutmann, R. J., and Cale, T. S., 2005, "Thermal Stresses in 3D IC inter-wafer Interconnects," Elsevier Journal of Microelectronic Engineering, Vol. 82.
- [11] Selvanayagam, C., Lau, J. H., Zhang, X., Seah, S. K. W., Vaidyanathan, K., and Chai, T. C., 2009, "Nonlinear Thermal Stress/Strain Analyses of Copper Filled TSV (Through Silicon Via) and Their Flip-Chip Microbumps," *IEEE Trans. Adv. Packag.*, **32**(4), pp. 720–728.
- [12] Dixit, P., 2008, "Numerical and Experimental Investigation of Thermomechanical Deformation in High-Aspect-Ratio Electroplated Through-Silicon Vias," *J. Electrochem. Soc.*, **155**(12), pp. H981–H986.
- [13] Wang, X., and Yin, W., 2010, "Multiphysics Characterization of Transient Electrothermomechanical Responses of Through-Silicon Vias Applied With a Periodic Voltage Pulse," *IEEE Trans. Electron Devices*, **57**(6), pp. 1382–1389.
- [14] Wakil, J., 2010, "Thermal and Mechanical Analysis of Interconnect Structures in 3D Stacked Packages," Ph.D. Dissertation, University of Texas, Austin.
- [15] Kovalenko, A. D., 1969, *Thermoelasticity* Wolters-Noordhoff Publishing Groningen, The Netherlands, Chaps. 1–2.
- [16] Chen, J., and De Wolf, I., 2002, "Raman Spectroscopy as a Stress Sensor in Packaging: Correct Formulae for Different Sample Surfaces," Proceedings, ECTC.
- [17] De Wolf, I., and Maes, H. E., 1996, "Stress Measurements in Silicon Devices Through Raman Spectroscopy, Bridging the Gap Between Theory and Experiment," *J. Appl. Phys.*, **79**(9), pp. 7148–7156.
- [18] Stevenson, M. E., Jones, S. E., and Bradt, R. C., 2003, "The High Strain Rate Dynamic Stress-Strain Curve for OFHC Copper," *Mater. Sci. Res. Int.*, **9**(3), pp. 187–195.
- [19] Bose, A., Sims, D., and German, R. M., 1988, "Test Temperature and Strain Rate Effects on the Properties of a Tungsten Heavy Alloy," *Metall. Trans. A*, **19A**, pp. 487–494.