

## Large-area patterning of a solution-processable organic semiconductor to reduce parasitic leakage and off currents in thin-film transistors

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We describe two techniques for patterning spin-cast thin films of a solution-processable organic semiconductor, triethylsilylethynyl anthradithiophene (TES ADT), to eliminate parasitic leakage currents and to lower off currents in thin-film transistors. One technique utilizes UV light in the presence of solvent vapors to simultaneously define the active channel and to crystallize TES ADT. The second technique selectively removes TES ADT from the nonchannel regions of the thin-film transistors through direct contact with a poly(dimethylsiloxane) stamp. Both patterning techniques yield thin-film transistors with high charge-carrier mobility ( $\geq 0.1 \text{ cm}^2/\text{V s}$ ), low off currents ( $10^{-10}$ – $10^{-11}$  A), and minimal parasitic leakage. © 2007 American Institute of Physics.

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Over the past several decades, significant research has been focused on the materials development of organic semiconductors that exhibit high charge-carrier mobility when incorporated in thin-film transistors. For example, organic thin-film transistors with pentacene<sup>1–4</sup> and derivatives of polythiophene<sup>5,6</sup> active layers routinely exhibit charge-carrier mobilities exceeding  $0.1 \text{ cm}^2/\text{V s}$ ; such mobilities satisfy current requirements for backplane circuitry to drive pixels in flexible active-matrix displays.<sup>7–9</sup> Improving the charge-carrier mobility alone, however, is insufficient for realizing high-performance organic thin-film transistor arrays. In addition to high charge-carrier mobility, applications-relevant organic thin-film transistors should exhibit negligible parasitic leakage currents to minimize electrical cross-talk between neighboring devices; they should also exhibit low off currents to maximize contrast between the on and off states.<sup>7,10,11</sup> To eliminate parasitic leakage currents and to minimize off currents in high charge-carrier mobility devices, the organic semiconductor must be patterned to constrain the charge carriers to the transistor channel. Several techniques exist for patterning vapor-deposited organic semiconductors, such as direct evaporation through a shadow mask,<sup>4,12</sup> and derivative photolithography techniques that do not damage the organic semiconductor.<sup>11,13,14</sup> To take advantage of the low-cost solution deposition techniques, such as spin casting and drop casting, which indiscriminately deposit the organic semiconductor across the substrate, straightforward methods for patterning<sup>15–19</sup> solution-processable organic semiconductors<sup>20–25</sup> after they are deposited need to be developed.

Here, we report two techniques for patterning a solution-processable organic semiconductor, triethylsilylethynyl anthradithiophene (TES ADT),<sup>21,22,26</sup> post-spin-casting over large areas. TES ADT is a *p*-type, small-molecule organic semiconductor that is electrically active as synthesized.<sup>22</sup> In a previous publication, we demonstrated that thin-film transistors containing spin-cast TES ADT, which are subsequently crystallized in 1,2-dichloroethane vapors at ambient conditions, routinely exhibit charge-carrier mobility of  $0.1 \text{ cm}^2/\text{V s}$ .<sup>26</sup>

To eliminate parasitic leakage and reduce off currents, we patterned TES ADT by selective UV light illumination in the presence of solvent vapors to define the active channel region in the TES ADT thin-film transistor and to simultaneously crystallize the amorphous TES ADT. Alternatively, we can also use poly(dimethylsiloxane) (PDMS) stamps<sup>27</sup> to selectively remove TES ADT from the nonchannel regions of TES ADT thin-film transistors. To demonstrate these patterning techniques, we built bottom-contact thin-film transistors on a silicon-silicon dioxide platform with spin-cast TES ADT. Highly doped silicon served as a common gate electrode for all the transistors on the same chip, and a thermally grown silicon dioxide (100 nm) served as the gate dielectric. Gold source and drain electrodes (40 nm) were deposited on the dielectric surface through a shadow mask using electron-beam evaporation. Following electrode deposition, the chip was placed in an UV/ozone chamber for 10 min. TES ADT solution (2 wt % in toluene) was then spin coated directly on the UV/ozone treated surfaces yielding a 100 nm thick amorphous TES ADT film. The fabricated transistors had a channel length of 100  $\mu\text{m}$  and a channel width of 1000  $\mu\text{m}$ .

To pattern with UV irradiation, the TES ADT-coated silicon chip is placed in a sample holder in the presence of a few

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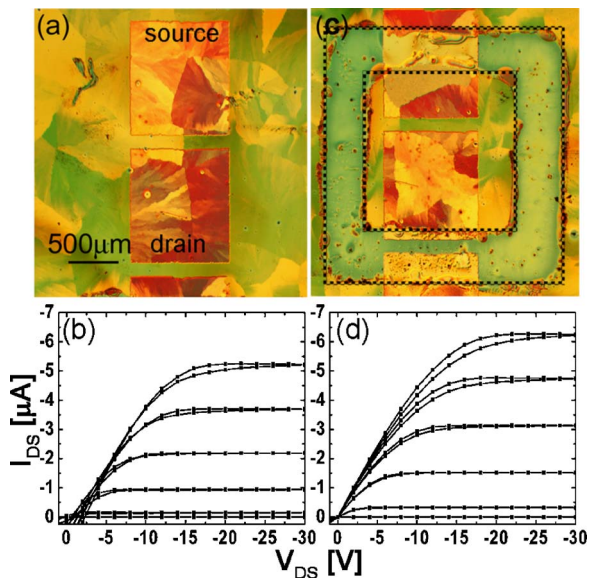


FIG. 1. (Color online) (a) Optical micrograph and (b) current-voltage characteristics for an unpatterned but separately crystallized TES ADT thin-film transistor with a charge-carrier mobility of  $0.10 \text{ cm}^2/\text{V s}$  and off current of  $10^{-10} \text{ A}$  and (c) an optical micrograph and (d) the current-voltage characteristics of a TES ADT thin-film transistor patterned with UV light having a charge-carrier mobility of  $0.12 \text{ cm}^2/\text{V s}$  and an off current of  $10^{-11} \text{ A}$ . In both transistors,  $L=100 \text{ }\mu\text{m}$  and  $W=1000 \text{ }\mu\text{m}$ .

drops of 1,2-dichloroethane. The nonchannel regions on the chip are then selectively irradiated with 365 nm UV light at  $540 \text{ mW}/\text{cm}^2$  for 1–2 min. We used an EXFO Omnicure UV curing system equipped with a Texas Instruments digital micromirror<sup>28</sup> array device for parallel light modulation in these experiments. In the irradiated regions, TES ADT dewets the substrate; this dewetting process can be monitored by a color change in the illuminated regions. Simultaneously, TES ADT crystallizes in the presence of dichloroethane vapors in the nonirradiated channel regions of the transistors. We note that this selective dewetting only occurs with amorphous TES ADT in the presence of dichloroethane vapors. In the absence of any organic solvent vapors, the molecules are not sufficiently mobile to rearrange on the substrate surface. This dewetting process is driven by surface energy differences between the substrate and TES ADT. As the molecules are plasticized by dichloroethane vapors, the thermal energy provided by UV illumination in the irradiated regions allows TES ADT to migrate from the substrate surface to the neighboring TES ADT surface. UV-visible near-infrared spectroscopy experiments carried out on solutions and thin films of TES ADT before and after illumination reveal identical spectra, indicating that TES ADT is not photobleached or degraded during the illumination process.

During patterning, TES ADT simultaneously crystallizes due to the presence of dichloroethane vapors in the unirradiated regions.<sup>26</sup> Consequently, we can crystallize TES ADT in the channel and remove it from the nonchannel regions of the transistor in a single processing step to yield TES ADT thin-film transistors with high charge-carrier mobility ( $0.1 \text{ cm}^2/\text{V s}$ ), low off currents ( $10^{-10}$ – $10^{-11} \text{ A}$ ), and negligible parasitic leakage currents. Optical micrographs of an unpatterned but separately crystallized transistor and a transistor patterned by selective UV illumination are shown in Figs. 1(a) and 1(c), respectively. The irradiated region of the patterned thin-film transistor has been highlighted in Fig.

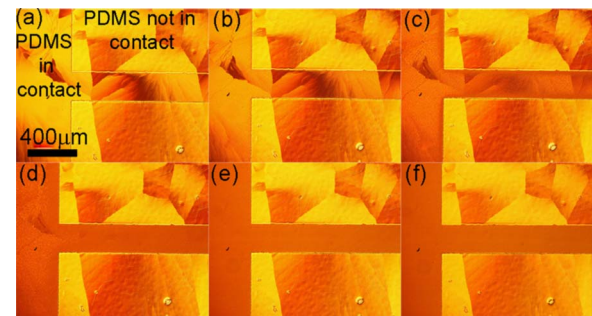


FIG. 2. (Color online) Optical micrographs of TES ADT viewed through a PDMS stamp (a) on initial contact, (b) after 30 min, (c) 1 h, (d) 3 h, (e) 6 h, and (f) 12 h of contact.

1(c) for clarity. In both micrographs, TES ADT is highly crystalline, as evinced by the birefringence from neighboring grains. The corresponding current-voltage characteristics for each of the transistors are shown in Figs. 1(b) and 1(d), respectively. While the charge-carrier mobilities of the patterned and unpatterned transistors are comparable, at  $0.1 \text{ cm}^2/\text{V s}$ , the parasitic leakage currents that are evident at low source-drain voltages in the unpatterned transistor [Fig. 1(b)] are eliminated in the patterned transistor [Fig. 1(d)]. Additionally, the off current is reduced by an order of magnitude in the patterned transistor ( $10^{-11} \text{ A}$ ).

The second technique for patterning TES ADT uses a PDMS stamp to selectively remove TES ADT from the nonchannel regions of the thin-film transistors. The PDMS stamp is created by casting and curing a PDMS prepolymer (Sylgard 184, Dow Corning) against a previously patterned, photolithographically defined silicon master.<sup>29,30</sup> The stamp geometry was chosen such that the recessed regions define the transistor channels. Patterning of TES ADT is accomplished by contacting the PDMS stamp against precrystallized TES ADT thin-film transistors. Specifically, TES ADT is removed through selective diffusion into the PDMS stamp in the regions of direct stamp and substrate contact (the nonchannel regions). Diffusion of TES ADT into PDMS is a surprising result given that the diffusing species is a crystalline solid. Evidence of diffusion of crystalline TES ADT is shown in Fig. 2. This series of optical micrographs are taken through the PDMS stamp, while it remains in contact with the crystalline TES ADT thin film. Specifically, Fig. 2(a) shows the crystalline TES ADT film immediately after it is contacted with a patterned PDMS stamp. The rectangular regions of the image correspond to the recessed regions of the PDMS stamp in which TES ADT is not in direct contact with PDMS. As time progresses [Figs. 2(b)–2(f)], TES ADT diffuses into the PDMS stamp and we observe a corresponding loss of crystallinity in the regions of stamp-substrate contact. After approximately 6 h [Fig. 2(e)], TES ADT has completely diffused from the silicon dioxide surface into the PDMS stamp in the regions of contact. TES ADT, however, remains crystalline in the regions of noncontact.

The patterned TES ADT thin-film transistors retain their high charge-carrier mobility ( $0.15 \pm 0.05 \text{ cm}^2/\text{V s}$ ), but now they exhibit virtually no parasitic leakage currents [Fig. 3(a)], and have low off currents ( $10^{-10}$ – $10^{-11} \text{ A}$ ). In contrast, unpatterned but separately crystallized TES ADT thin-film transistors exhibit off currents ranging from  $10^{-6}$  to  $10^{-9} \text{ A}$ . As the amount of TES ADT removed from the nonchannel regions of the thin-film transistors increases, the off currents

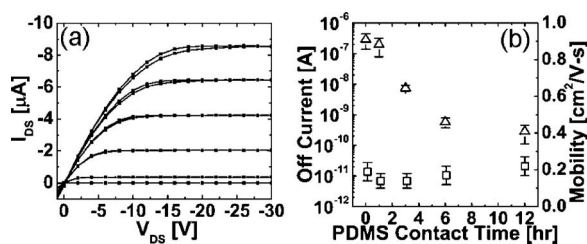


FIG. 3. (a) Representative current-voltage characteristics for a patterned, crystalline TES ADT thin-film transistor after 1 h of contact with a PDMS stamp. (b) The off current ( $\Delta$ ) decreases, while the mobility ( $\square$ ) remains constant with contact times.

of the thin-film transistors decrease correspondingly. The off current is plotted as a function of PDMS contact time in Fig. 3(b). After 1 h of contact time, the off current remains high, as would be expected given the incomplete removal of TES ADT seen in Fig. 2(c). The off current continues to decrease with increasing PDMS contact time. After 12 h of PDMS contact, the measured off currents are on the order of  $10^{-10}$  A in the patterned transistors, which are significantly less than the off currents ( $10^{-7}$  A) measured in the same transistors prior to patterning. Since the on currents remain the same before and after patterning, we observe comparable mobilities and a net increase in the on/off current ratio in the postpatterned thin-film transistor, implying that the integrity of TES ADT in the transistor channel is not compromised by the patterning process.

For any organic semiconductor patterning technique to be utilized on a commercial scale, the technique must be amenable to patterning large arrays of transistors. Both the selective UV illumination and the PDMS stamp patterning techniques can be scalable for patterning arrays of high-performance thin-film transistors; demonstrations with arrays comprising three and eight devices are shown in Figs. 4(a) and 4(b), respectively. The charge-carrier mobilities of the transistors patterned by selective UV illumination and with PDMS stamps are at least  $0.1 \text{ cm}^2/\text{V s}$ , the parasitic leakage currents have been eliminated, and the off currents are  $10^{-10}$  A or less. Currently, the size of the transistor array patterned by selective UV illumination [Fig. 4(a)] is limited by the aerial projection of the light source ( $2 \times 2 \text{ mm}^2$  maximum illumination area). This limitation, however, can easily be overcome by increasing the size of the projection system or by utilizing a moving light and solvent reservoir to accommodate a semicontinuous patterning process. In the case of patterning with PDMS stamps, larger stamps can be utilized for large-area patterning. For example, a  $5 \times 5 \text{ in.}^2$  PDMS stamp has been successfully used to define gold source and drain electrodes by microcontact printing for an array of 256 pentacene thin-film transistors.<sup>31</sup>

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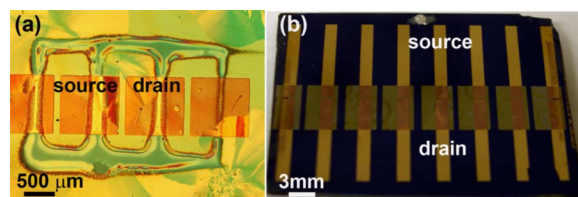


FIG. 4. (Color online) (a) Optical micrograph of an array of three thin-film transistors patterned with selective UV light illumination. (b) Image of an array of eight thin-film transistors patterned with 12 h of contact with a PDMS stamp.

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